Focus sur les activités fiabilité et Grand Gap

Présentation des projets en lien avec PROOF et perspectives pour une réflexion de structuration de l’écosystème électronique de puissance dans la région et en France

COS – PROOF
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Responsible of the “High Reliability” Center of Competence
OUTLOOK

- Introduction: Context and Objective
- Overview of WBG activities for Power Electronics
- Focus SICRET:
  - From PoF to better test, better Design, (and better manufacturing)
  - Identification and deployment of the R&T program (beyond Q101, JEDEC)
  - Focus on collaboration with LAAS

- Conclusion and Perspectives
IRT-Saint Exupery Model

Cofinancé par les membres industriels & l’État dans le cadre du PIA*

*Le Programme d’investissements d’avenir

Catalyse  →  Accélération  →  Transfert
High Reliability Center of Competence: Overview

Bridging (COTS\textsuperscript{(1)} based on) emerging technologies to harsh environment operation

Reliability based on PoF analysis
(from component/cell to board/stack level)

- Comprehensive Risk (Lifetime & CFR) assessment methodology (FRAME)

Natural Radiation immunity
- Radiation induced failure mechanisms analysis and understanding

Electromagnetic Compatibility (EMC) from NFS to System
- Obsolescence management
- Fast Board prototyping and tool development for optimization / verification

\textbf{GOALS !! Objectives}

- Predictive / Diagnostic Reliability
- Wear-out / Obsolescence Management
- Fast Prototyping (tools)
- Qualification / Certification support

\textbf{Means Toward sustainable IRT}

\textbf{Advanced Know-how + Expertise}

\textbf{Cost-effective Methodologies}

\textbf{New Guidelines}

\textbf{Innovative Platforms}

\textbf{Predictive / Diagnostic Reliability}

\textbf{Wear-out / Obsolescence Management}

\textbf{Fast Prototyping (tools)}

\textbf{Qualification / Certification support}

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\textsuperscript{(1)} Semiconductors components (Deep Sub Micron (FDSOI, FinFET, 3D), WBG based transistor (GaN and SiC)...) and Electrochemical for energy sources/storage (Fuel cell, Li-X batteries, Supercapacitors); Assembly and packaging solution (High Power, High Density, High Frequency) SoC or SiP.
Components / Functions

Roadmap

More
Electrical Power (propulsion / non propulsion)
Switches/Transistors
Battery, Supercap. Fuel cell
Intercon. / Assembly

More DIGITAL functions
FPGA µProcessor - µController
Memory (DDR, FLASH, ...)

Silicon
- Bulk CMOS
- Fin FET
- FD - SOI
- Si and III-V GAA
- GaN
- Li-Ion, Li-Alloy, Li-S, Li-Polymer, Li-Solid
- Li-air (?)

Reliability based PoF Analysis and Modeling (component to board level)

FM Analysis and understanding

Innovative Methodologies & Tools (Test and Design)

Electromagnetic Compatibility (EMC) behavior (component to board)

EMC models from components to equipment

Experimental Tool development and Optimization

Natural Radiation Immunity based on experiments and models

Radiation induced failure mechanisms analysis and understanding

Innovative Methodology and Tool

End of Moore’s Law ???

New 2D Materials (TMD, ...?)

Switches/Transistors

Silicon Fin-FET

Si and III-V GAA

Li-Ion

Li-Alloy, Li-S, Li-Polymer, Li-Solid

Li-air (?)

Li-ion

Battery, Supercap. Fuel cell

QFN, BGA

FC-BGA

FD-SOJ

WLP

Si and III-V GAA

SiP

3DIC

Reliability (CFR / EOL) / Obsolescence Management

Fast / Virtual Prototyping (DfR, EMC compliance, Technology Eval.)

Certification Support

Objectives

Predictive / Diagnostic Reliability

End of Moore’s Law ???
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Power Drive Systems

Use of SiC and GaN

Source: Projects Integration, EPowerDrive

Increasing Switching Frequency

- High CM Current
- Heavy/bulky CM Filters

Increasing Switching Speed

- High CM Currents
- Heavy/bulky CM Filters

- High overvoltage on motors
- Heavy/bulky DM Filters
Project WBG: Overview

* Example: Multiple-Stage Flying-Cap Three phases 70KW 540V GaN (144 series & parallel) PCB Embedded Inverter (with reduced CEM passive integration) → IRT-Projects: ePowerdrive
Integration in Complex Systems

Multiple-Stage Flying-Cap Three phases 70KW 540V GaN (144 series & parallel)

- How to take into account the drift of key parameter e.g. Vth
- How to discriminate between die and higher complex integration level failures
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Need of reliability insight at semiconductor (die) level


How to discriminate between reversible (recovery) and not reversible phenomena (aging)!!

Lack of SC induced aging indicator!!
Need of reliability insight at semiconductor (die) level

How to discriminate between reversible (recovery) and not reversible phenomena (aging)!!

Need of reliability insight

GATE OXIDE RELATED DRIFT: Causes identification → Focus on the transition layer SiO₂/SiC

Background: Existing Patents on gate oxide growth (1/2)

Patent Number: 5,506,421
Date of Patent: Apr. 9, 1996
Patent No.: US 6,246,076 B1
Date of Patent: Jun. 12, 2001
WO 02/29900 A2 2002

The mechanism of defect creation and passivation at the SiC/SiO₂ interface

Peter De´ak1, Jan M Knaup1, Tam´as Hornos2, Christoph Thill1, Adam Gall2 and Thomas Frauenheim1

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2 Budapest H-1521, Hungary

Source: European project (MobiSiC) on NIT improvement by passivation process (N₂O, NO)

Source: KAKENHI Grant No. 15H03969 (Japan)


Dielectric trap relaxation) → Slow (far from SiO₂) to Fast (close to SiO₂)
Currently available SiC MosFET devices present Vth instability.

Without precaution, the inherent and “normal” Vth instability could blur Vth parameter drift related to device aging.

⇒ A robust Vth indicator is mandatory for reliability studies.

We have optimized a Vth measurement technique that ensures:

- independent of previous device normal-operation-history
- almost perfectly reproducible Vth value, that is based on:
  - device preconditioning-sequence
  - perfect measurements timing-control.

While standard measurement technique could lead to several hundred of mV Vth instability, depending on previous device operating-conditions, our technique reduces this variation to a few mV range.

D. Tremouilles
D. Hachem (PD-IRT)
Influence of pre-conditioning on Vth measurement

Influence of Tfloat

Pre-conditioning robustness against device “normal operation history”

<table>
<thead>
<tr>
<th>Pre-conditioning Method with tfloat=0</th>
<th>ΔVth-pos (Positive Stress of 20s)</th>
<th>ΔVth-neg (Negative Stress of 20s)</th>
<th>Vth (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive only</td>
<td>77 mV</td>
<td>144 mV</td>
<td>3.19</td>
</tr>
<tr>
<td>Negative + Positive</td>
<td>1 mV</td>
<td>14 mV</td>
<td>3.15</td>
</tr>
</tbody>
</table>
Influence of pre-conditioning on Vth measurement

➢ Open questions

- What is the real Vth behavior during application use case: with switching, with off time,…? What is permanent drift?
  How hysteresis is evolving during use case?

- What is impact of Vth variations on conduction (RDSon/leakage) and switching losses?

- How this phenomenon affects behavior of components in parallel or in series? Is Vth the proper parameter for selection of components used in parallel?

D. Tremouilles
D. Hachem (PD-IRT)
Need of reliability insight


Lack of SC induced aging indicator !!
Lack of SC induced aging indicator!!
Need of Characterization Tools & Methods

NEED of investigation technique / Approach

→ LFN based technique!

WANG et al.: TRAP ANALYSIS BASED ON LFN FOR SiC pOWER MOSFETs UNDER REPETITIVE CIRCUIT STRESS

Lack of aging indicator

the $S/I^2$ at 10 Hz versus $I_{ds}$ for the fresh device, 200 and 500 SC cycles device, respectively.
Future electrification technologies will require drastic improvements of power electronics, with higher power density & efficiency, but without negative impact on Reliability.

SiC Wide Bang Gap (WBG) technologies will be key enablers thanks to their higher electrical performances (at 1200V toward 3300V)

However not enough knowledge and standards test allowing their introduction exist → High Risks !!!
Project Structure

END USER (Multi-sector) NEEDs

AERO (Liebherr, SafranTech, Safran Elect. &Power)
AUTO (Vitesco, ...)
RAILWAY (Alstom)
STATIONARY (Supergrig)

Typ. Working Conditions (MPs)

Reliability Set-up / Expertise
Scientific / Technical Offer (Laboratories):
AMPERE (Lyon)   ALTER Tech. (Toulouse)
IES (Montpellier) NUCLETUDES (Paris)
LAAS (Toulouse)   ITE-Supergrid (LYON)
LAPLACE (Toulouse) DGA* (French MoD)

DUTs
- MV (STM)*
- HV (MITSUBISHI) *

Collaboration Agreement
Collaboration/Purchase Agreement
Purchase

Others COTS providers (Wolfspeed, Infineon ROHM,...)

AEC-Q

4 (18MM) Post Doc hired at 4 laboratories + 4 PD supervisors
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### Project WBS: SiCRET vs SiCRET+

#### Reliability Analysis and Test methodology Development and Validation (on DUT1 → STM)

#### Qualification Test plan Definition (Proposal)

#### Guidelines definition (SOA, Design rules, …)

#### Test Methodology application (on DUT2 and DUT3)

#### Test Methodology application (on DUT4 and DUT9)

#### Reliability Analysis and Test methodology Development and Validation (On MUT1)
Projest Status and Perspectives

- Establish a reference body of knowledge (database DUT for Automotive usage profile) of

Qualification Test plan Definition (Proposal)

Guidelines definition (SOA, Design rules, …)

At Power Module level including other studies/tests.
  - Low pressure, humidity,
  - Thermal management (power cycling, temperature cycling)
  - EMC emission/immunity

Enhanced by the collaboration with STM (associate Partner of the project)

Source: ST Microelectronics
GaN Wide Bang Gap (WBG) technologies will be key enablers

However not enough knowledge NOR “proven-in-use” and standards test allowing their introduction exist → High Risks !!!
Main Challenges:
- PoF not-well understood / established
- Panoply of (not mature) technologies (e/d mode)
- Design rules and test protocol for advanced (embedded) packaging

Application domain:

Project Rational:

TENTATIVE: BUDGET: TBD M€ - DURATION: 36MM Start Date: 2021-Q2
Major Challenges wrt SiC

Lack of standard packaging

Many technological choices

The landscape is populated by many providers (SME often fabless) using large foundries with established Silicon legacy!
Exploitation and Lighthouse Activities

- **Consolidation** of a reliability and risk assessment tool (capitalization)
- **Structuring** National reliability network (CFF, NRTW, …)
- **Supporting** international standardization (JEDEC, EIC, JEITA, …)
- **Connecting** with major international players/networks (AEC, ECPE, CPES, …)
CONCLUSIONS

- Need to identify and characterize “indicators” observables” by PRECISE, REPRODUCIBLE, ROBUST methods
- Need to understanding about underlying PoF based on above “indicators” observable”
- NEED of investigation technique / Approach by specialized platforms dedicated to WBG

Example: SICRET project

- Inverter Test with Aceler. Switch. Conditions
  - H. Morel
  - H. Hamad (PD)
- Short Circuit Induced phenomena
  - F. Richardon
  - Y. Barazi (PD)
- Cosmic Radiation induced phenomena
  - A. Touboule
  - H. Rizk (PD)
- Other specific phenomena

Gate Oxide Related Phenomena Characterization & Understanding (PROOF)

D. Tremouilles
D. Hachem (PD)
H. Morel
H. Hamad (PD)
F. Richardon
Y. Barazi (PD)
A. Touboule
H. Rizk (PD)
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Merci de votre attention