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Study of GaN HEMTs Robustness to Application-Like, Software-Controlled Overshoots Emulating Different Gate Routings in Original 50 Ohms Environment

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***Abstract*—In the field of transient tolerance tests, few studies have been conducted on gate voltage spikes of GaN HEMT components. A parametric generation of such overvoltage either implies precise and tedious hardware gate circuitry design, or require some simplification of the waveform making it less representative of actual and practical cases.**

Such tests will be easier to conduct thanks to the original 50 Ohms environment setup proposed in this work. This original test bench improves usual measurement bandwidths. It also allows spatial isolation of a tested device with its driver and power circuits (e.g. over one meter), limiting their complex interactions.

As a first demonstration of the setup capability, the breakdown overvoltage of a p-GaN HEMT is determined. Several gate voltage overshoots as high as twice the DUT nominal rating are then demonstrated not to degrade the tested device. Moreover, allowing such overshoots may enable to significantly reduce switching losses.

***Index Terms*—GaN, Overshoot, Transient, Spike, Deported Control, 50 Ohm Environment, Robustness, characterization**

Symbol Definition

- s is the Laplace variable;
- $\underline{f}(s)$ is the Laplace transform of f(t);
- $H(t)$ is the Heaviside function;
- $H_T(t) = H(t - T)$.

I. Introduction

Wide BandGap (WBG) devices display better behavior than Si devices regarding power and volume efficiency for static converters. GaN High Electron Mobility Transistors (HEMTs) enable higher working frequencies and reduced switching losses. Thus, smaller passive components are needed as filters in power applications. However, fast switching tend to trigger parasitic oscillations in both gate and drain circuitry. These oscillations result from the complex interaction of the inductive and capacitive behaviors of the components, circuits, and parasitics. They can lead to energy losses and failures. Equivalent models are proposed in literature [1], but identification of their parameters from actual PCBs is complex. Therefore, precisely predicting oscillations is much more difficult than modeling experimental ones. In particular, overvoltage studies require the generation of reproducible, precisely controlled and measurable OVSs. This entails either tedious PCB design, or the use of simpler waveforms, making them less representative of actual cases.

This work presents a generic characterization-setup design with full control of a power component state and its circuit parasitics. To do so, concepts from the radiofrequency transmission line model, and their application to move away a GaN HEMT from its command and power circuits are presented. A setup achieving high-frequency bandwidth is proposed along with its theoretical analysis. Several OVS robustness tests are conducted as a demonstration of the performances of the setup.

In section II, the origins and typical waveforms of gate OVerShoots (OVSs) are explored and compared to the existing literature of OVS robustness studies. The proposed setup and the underlying theoretical background is presented in section III. Experimental results are discussed in section IV.

II. GaN HEMTs Gate Overvoltages: Origins, Characterization, Consequences

Several phenomena can lead gate-source (or source sensing, if applicable) to hazardous voltage ringing and overshoots. Depending on the amplitude of the oscillations, the component is degraded at varying speeds [2]. An application-scale consequence is the false turn-off; upon switching on, the gate voltage oscillates lower than its threshold, causing undesired, partial switching [3].

Firstly is discussed typical origins and waveforms of gate OVS. Then, in the second part is a review of existing gate OVS robustness characterization methods.

A. Origins and Consequences of Gate Overshoots

GaN transistors feature intrinsic fast switching speed and excellent radiation tolerance. However, while fast transient are beneficial regarding the decrease of switching losses, the

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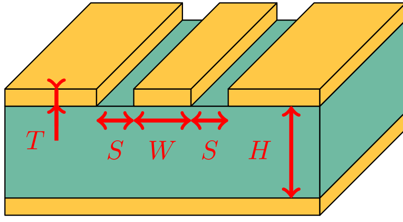


Fig. 1: A typical copper track section on a FR4 power PCB. $H = 1.5\,\mathrm{mm}$, $S = 0.15\,\mathrm{mm}$, $W = 0.2\,\mathrm{mm}$, $T = 35\,\mathrm{\mu m}$. $\epsilon_r = 4.5$, $\epsilon_{r,effective} = 2.20$. S and W are defined accordingly to EPC GaNs gate pads.

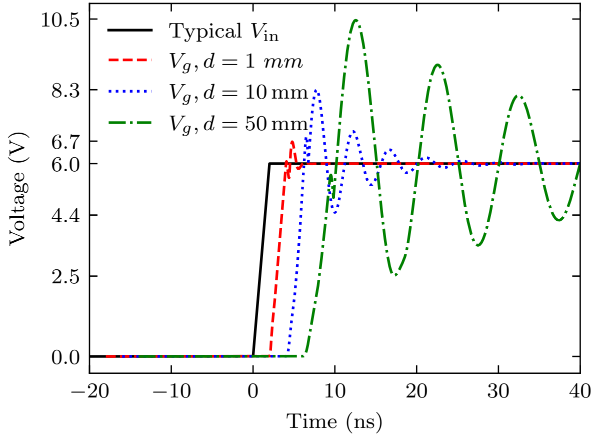


Fig. 2: Simulation: influence of the length of the gate copper track, time shifted for visual clarity. The modeled track is described in Fig. 1. Without parasitics, $V_g = V_{\text{in}}$.

parasitic RLC of the surrounding circuits are all the more excited by the high frequency content of the waveforms, creating oscillations jeopardizing the components.

Copper tracks alone provide enough inductance to create oscillations. A typical copper track section is presented in Fig. 1. According to [4], this section creates a linear inductance $L_l = 0.4\,\mathrm{nH\,mm^{-1}}$.

As an example, the effects of the length of the copper track between a typical driver and a p-GaN HEMT GS-065-004-1-L gate are simulated in Fig. 2; the longer the track, the higher its inductance and the higher the perturbation on the gate signal. Indeed, the track inductance resonates with the transistor gate-capacitance, creating oscillations that can be modeled by a 2nd or 4th order oscillator [1]. This is the reason why it is common to reduce the length of copper tracks to achieve better signal [5].

Furthermore, gate signal distortions may have many other origins like radiated coupling of adjacent tracks, especially power signal tracks. Perturbations from other parts of a circuit can also propagate through power supplies and tracks. These perturbations can in turn resonate with the presented equivalent LC circuitry.

B. Robustness Characterization

Since overshoots can occur in the most common converter designs, as shown in Part. II-A, it is essential to quantify the robustness of GaN HEMTs to those overshoots.

Several setups allow studying GaN gate robustness.

DC studies are the most straightforward to conduct since LC elements does not interfere in this case. The gate DC Breakdown Voltage (BV) of GaN HEMTs is thus generally provided in all device datasheets.

He et al. [6] present a study between stepped DC and pulsed test, which progressively steps up a DC stress applied at $100\,\mathrm{kHz}$, with $50\,\%$ duty cycle, until failure.

A setup approaching the typical waveforms presented in Part. 1 was designed by Wang et al. [2] [7], to find that gate overshoot robustness can be fitted with both lognormal and Weibull distribution. This design lets an inductance be charged upon a controlled level, to then discharge it in the gate of a GaN transistor. The inductance and gate capacitance then produce ringing similar to the expected realistic waveform but around $0\,\mathrm{V}$.

OVS robustness studies are less common than DC ones due to the strong impact of the circuitry on the gate signals. To perform parametric testing, the waveforms applied must be precisely controlled, and there must be no parasitics due to, nor in the measurement path. Since only few millimeters of copper tracks suffice to create parasitics for fast transient signals, the resulting gate and measurement circuitry must be dense; its conception is therefore tedious. With GaN packages of different sizes and shapes, redesigning optimized test-PCBs can be time-consuming.

Moreover, while dense PCB design allows for the reduction of parasitic inductances, it makes impossible to apply an environmental stress to the device only, rising the need for robust and costly circuits for each device, and hampering any efforts to study GaN environmental reliability.

III. Proposed 50 Ohm Setup

A common solution for parasitic management at any length of conductors is controlled impedance. This concept is based on transmission lines equations, which is standard in the field of radio-frequency.

The proposed 50 Ohms circuitry is presented in the following parts. The transmission line theory completely encompasses the lumped impedance approach developed in Part. II-A, but is fairly different in its calculations and reasoning. Therefore, it is presented in the following parts independently of the lumped-model approach.

A. Transmission Lines: Selected Theoretical Elements

While lumped elements are a valid model for the propagation of electromagnetic signals in conductors of small length compared to the signal spatial wavelength, the tools provided by the transmission line model are valid for any length of cable.

A set of two conductors part of a current loop is defined by two main parameters in the transmission line model:

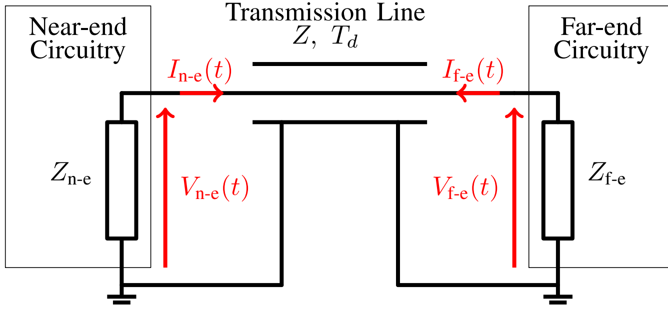


Fig. 3: Parameters of a transmission line and its environment.

- its characteristic impedance Z;
- the travel time of an electromagnetic signal across the length of the conductor T_d.

A circuit containing a transmission line can be described with the following set of parameters, schematized in Fig. 3):

- the transmission line, defined by its Z and T_d;
- the output impedance of the near-end side of the transmission line $Z_{\text{n-e}}$;
- the input impedance of the far-end side of the transmission line $Z_{\text{f-e}}$.

These elements allow calculating the near-end and far-end reflection coefficients:

$$\mathcal{R}_{\text{n-e}}(s) = \frac{Z_{\text{n-e}}(s) - Z}{Z_{\text{n-e}}(s) + Z}\ ;\ \mathcal{R}_{\text{f-e}} = \frac{Z_{\text{f-e}}(s) - Z}{Z_{\text{f-e}}(s) + Z} \tag{1}$$

While Z is usually real, these coefficients can be complex depending on $Z_{\text{n-e}}$ and $Z_{\text{f-e}}$. Note that a reflection coefficient is null only if the termination impedance is equal to the line impedance.

With these parameters, the system can be analyzed as such:

- By replacing the transmission line with its characteristic impedance Z, the voltage across Z is calculated. This voltage is the incident voltage wave $V_{i,\text{n-e}}(t)H(t)$;
- This voltage wave travels across the transmission line. Upon arriving at the far-end, the voltage wave:

$$V_{i,\text{f-e}}(t) = V_{i,\text{n-e}}(t - T_d)H_{T_d}(t) \tag{2}$$

  is reflected. The reflected wave is defined by:

$$\underline{V_{r_1,\text{f-e}}} = \underline{V_{i,\text{f-e}}}\mathcal{R}_{\text{f-e}} \tag{3}$$

- This reflected voltage wave then travels back to the near-end and reaches it with a delay:

$$V_{r_1,\text{n-e}}(t) = V_{r_1,\text{f-e}}(t - T_d) \tag{4}$$

  This wave is reflected as $V_{r2,\text{n-e}}(t)$, defined by:

$$\underline{V_{r_2,\text{n-e}}} = \underline{V_{r_1,\text{n-e}}}\mathcal{R}_{\text{n-e}} \tag{5}$$

- Subsequent calculations of reflections can be made following this method. If set as in Fig. 3, the same relations apply for current calculations.
- At any time, the apparent voltage is defined by the sum of all the voltage waves defined previously:

$$\begin{cases} V_{\text{tot,n-e}}(t) = V_{i,\text{n-e}}(t)H(t) + \sum_{k=0}^{\infty} V_{rk,\text{n-e}}(t) \\ V_{\text{tot,f-e}}(t) = V_{i,\text{f-e}}(t) + \sum_{k=0}^{\infty} V_{rk,\text{f-e}}(t) \end{cases} \tag{6}$$

- The DC analysis of the currents and voltages of the circuitry are obtained with an infinite number of rebounds that converge to a stationary DC state; thus, they do not depend on T_d. They can be obtained for any T_d, especially $T_d = 0$.

B. *Global Description and Functioning of the Setup*

The proposed setup is presented in Fig. 4. Following are presented the parts of the setup: driver-side, power-side, measurements; and its advantages for efficient characterization.

1) Driver side: The gate of the DUT is interfaced with a $50\,\Omega$ interconnection, and a voltage probe. The far-end of the gate $50\,\Omega$ coaxial cable is connected to a $50\,\Omega$-output-impedance waveform generator, in order for the reflection coefficient (1) at this end to be null.

As illustrated in Fig. 5, for any incident voltage $V_i(t)$ sent through the line by the generator, one reflection $V_r(t)$ occurs on the DUT side and there is no further reflection on the generator, thanks to the null reflection coefficient on its side.

Applying the results of the previous section (III-A), the following parameters are defined:

- the cable is defined by its impedance $Z_c = 50\,\Omega$ and delay T_c;
- the input impedance of the DUT gate is Z_g, and the output impedance of the generator is $Z_{\text{gen}} = 50\,\Omega$;
- the reflection coefficient on the DUT side of the cable is therefore:

$$\mathcal{R}_{\text{gate}} = \frac{Z_g - Z_c}{Z_g + Z_c} \tag{7}$$

Then, the two voltage waves present at any time at the DUT gate are:

- the generator incident voltage V_i, with a delay T_c created by the cable:

$$V_{i,\text{DUT}}(t) = V_i(t - T_c)H_{T_c}(t) \tag{8}$$

- and the reflected wave V_r, defined by $\mathcal{R}_{\text{gate}}$ and $V_{i,\text{DUT}}$:

$$\underline{V_{r,\text{DUT}}} = \mathcal{R}_{\text{gate}}\underline{V_{i,\text{DUT}}} \tag{9}$$

These waves are represented in Fig. 4. The apparent voltage at the DUT gate is thus:

$$V_g(t) = V_{i,\text{DUT}}(t) + V_{r,\text{DUT}}(t) \tag{10}$$

Then, by combining (9) and (10):

$$\underline{V_g} = \underline{V_{i,\text{DUT}}}\,(1 + \mathcal{R}_{\text{gate}}) \tag{11}$$

Hence, any desired gate voltage can be obtained by generating the appropriate V_i defined by (11) and (7):

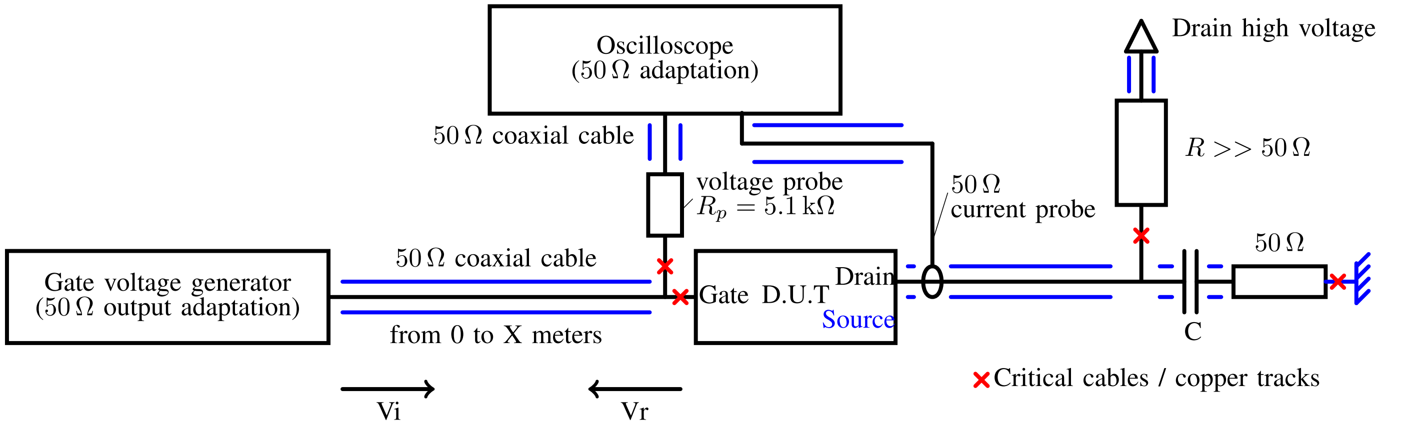


Fig. 4: Proposed 50 Ω setup. Each 50 Ω cable can be of arbitrary length, contrarily to the short critical paths.

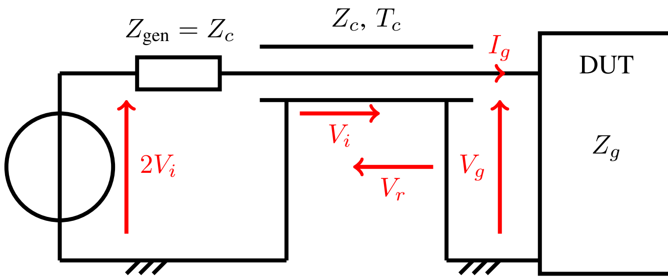


Fig. 5: Gate circuitry model. With a Thevenin model for the waveform generator, V_i is generated with a $2V_i$ voltage source.

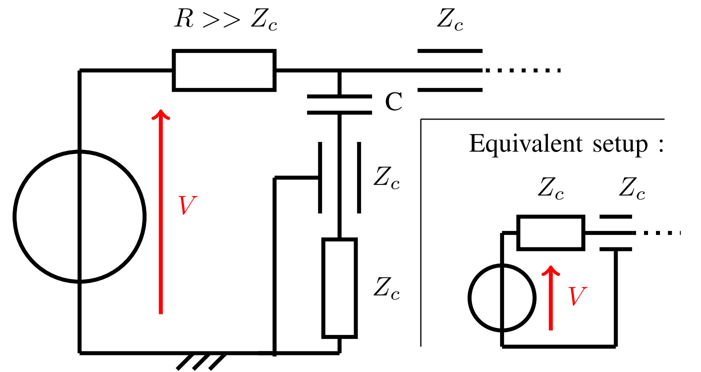


Fig. 6: Drain voltage generator circuitry.

$$\underline{V_{i,\text{DUT}}} = \underline{V_g} \frac{Z_g + Z_c}{2Z_g} \tag{12}$$

Since Z_g is highly non-linear and, in some cases, depends on the power circuitry as well as the DUT intrinsic properties, (12) can be rewritten as:

$$\underline{V_{i,\text{DUT}}} = \frac{\underline{V_g} + \underline{I_g} Z_c}{2} \tag{13}$$

Since $V_{i,\text{DUT}}$ is only a T_g-shifted V_i, V_i is entirely defined by V_g and I_g. Moreover, with Z_c being real, (14) is similar in time-domain:

$$V_{i,\text{DUT}}(t) = \frac{V_g(t) + I_g(t) Z_c}{2} \tag{14}$$

The reproduction of an in-application measured (V_g, I_g) is thus possible with the proposed setup. While V_g is usually measurable on PCBs, I_g can be obtained through simulation, knowing V_g.

As displayed in Fig. 5, a Z_c Thevenin voltage source providing $2V_i$ generates the appropriate V_i through the line.

In the following experiments, the theoretical V_i waveforms obtained by this method are synthesized thanks to a home-made generator. This waveform generator is currently in patenting process.

2) Power side: In the same way as in Part. III-B1, the drain of the DUT is connected to a cable of controlled impedance. This cable is terminated by the drain voltage generator, which is constituted of a high voltage source, a high value resistor R, a decoupling capacitor and an adaptation 50 Ω resistor. The drain voltage generator is represented in Fig. 6. This generator acts as a Z_C-adapted voltage source: the high resistor branch charges the capacitance and ensures the high-frequency stability of the voltage generator. Fast drain transients generated by the DUT are not reflected by the generator thanks to the capacitance and Z_c resistor.

The equivalent drain circuit is actually described by the same schematic as in Fig. 5, with Z_{DS} in place of Z_G. Eq. (14) can thus be rewritten as:

$$V_{i,\text{DUT}}(t) = \frac{V_{\text{DS}}(t) + Z_c I_{\text{DS}}(t)}{2} \tag{15}$$

Eq. 15 is equivalent to the circuitry in Fig. 7. Correspondence between Fig. 6 and Fig. 7 confirms that $V = 2V_i$. The power side circuitry thus behaves as in Fig. 7. Hence, even tho the generator is deported, the drain-source voltage behaves as if commuting on an adjacent resistive charge.

3) Critical signal paths: In order to eliminate all parasitic, all copper tracks or cable must be of controlled impedance.

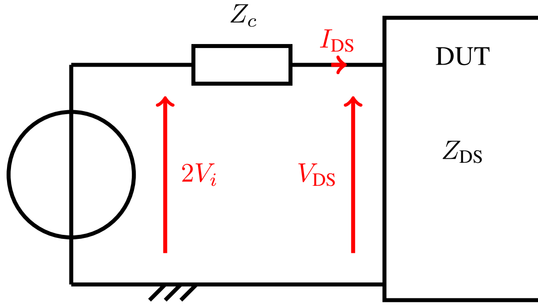


Fig. 7: Power side circuitry equivalent according to Fig. 6. As represented in Fig. 5, $2V_i = V$.

However, some signal paths must be as short as possible to prevent impedance discontinuity and unwanted signal rebounds. Those are marked with red crosses in Fig. 4.

- High value resistors, either for probing (R_p) or injecting small currents (R) must be as close to the main signal path as possible. If not, a signal travelling through the main line would be divided between its main track and this sub-path, with the sub-path termination not being adapted. Thus, rebounds would occur and be visible as parasitics on the main signal.
- Adaptation resistors must be connected directly to the ground. The rebounds and parasitic are as dampened as the ground paths are short.
- For voltage probing, the voltage probe must be as close as possible to the main line termination. If not, the delay δT between the probe and the line termination would be apparent in the measurement. In this later case:

$$V_{\text{probe}} = V_{i,\text{DUT}}(t + \delta T) + V_{r,\text{DUT}}(t - \delta T) \quad (16)$$

4) Experimental implementation and results: Several measurements are made to extract data using the proposed setup.

- The voltage probe allows monitoring V_g. As displayed in Fig. 7 and demonstrated in the corresponding calculations, a cable Z_c adapted at its termination behaves like a Z_c resistor. Thus, the oscilloscope voltage is $V_{\text{oscilloscope}} = \dfrac{50}{50 + R_p} V_{\text{GS}}$.
- The drain current probe is designed to keep the $50\,\Omega$ impedance and thus to avoid parasitic. Contrarily to the gate voltage probe that must be placed close to the gate, the position of the drain current probe on the line does not really matter. V_i is DC, so the time-shifting described by (16) only shifts the measurement in time without distorting it. This time-shift can be measured independently and compensated in the oscilloscope settings.
- The oscilloscope used for this series of experiment is a DSOS104A, with a 1 GHz bandwidth.

5) Advantages of the setup; Parasitics: By controlling the impedance of all interconnections, copper tracks inductances presented in part II-A are integrated in the calculations within the complete model of transmission lines. Therefore, there are no parasitics as long as the line impedance is controlled.

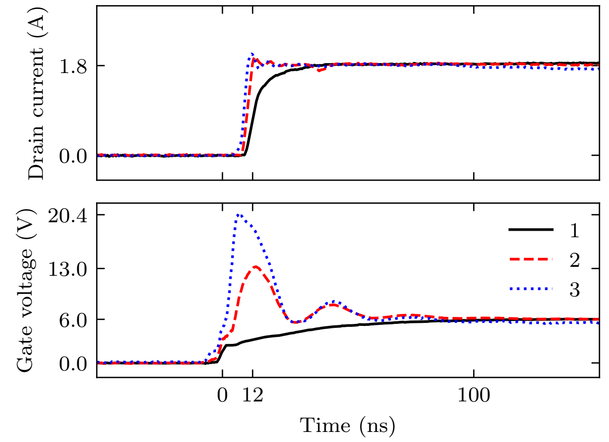


Fig. 8: Typical experimental waveforms applied to the gate to find its spike breakdown (22 V OVS). The drain switching energies are of 3.3 µJ (1) and 0.6 µJ (2).

However, electromagnetic coupling can still occur from the power side to the command side. This is prevented by only using well-defined, shielded sections, as in Fig. 1. These section have a well-defined impedance and the current loop is very small, due to the proximity of all conductors. $50\,\Omega$ cables are shielded and bring very little to no parasitics. Clean signal paths of controlled impedance are straightforward to route in this application due to the permitted long track length and small number of tracks. The only remaining source of parasitics is the interconnections or welds; these are however as small as the signal path through the welding is short, thus actually creating very little to no parasitics.

IV. Robustness Testing

Measurements were conducted with the proposed circuitry and a homemade gate voltage generator.

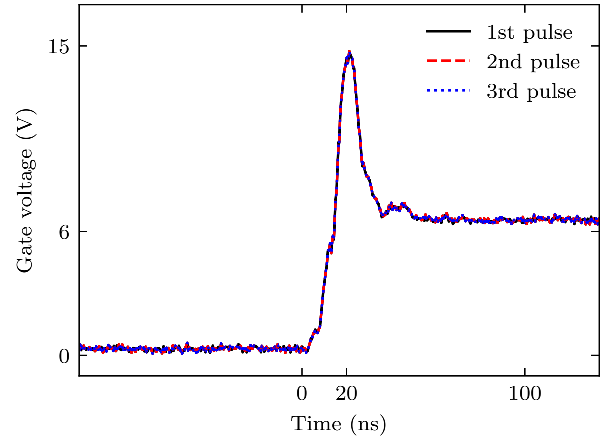


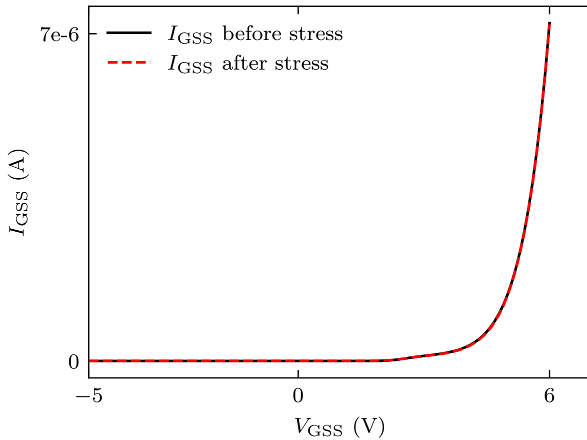
Fig. 9: Experimental stress waveforms. The excellent repeatability and low parasitics level of the generated waveforms are in line with the developped theoretical elements.

Firstly, p-GaN HEMTs GS-065-004-1-L were submitted to a wide range of OVS, as displayed in Fig. 8, to find their approximate dynamic Breakdown Voltage BV_{dyn}. Their apparent gate-source resistance was measured with an ohmmeter (Keysight U1241C) before and after each stress. The resistance was not measurable by the ohmmeter for an unbroken device (over $10\,M\Omega$). The breakdown voltage was found to be around $22\,V$ OVS, after which the measured resistance was around $7.5\,M\Omega$.

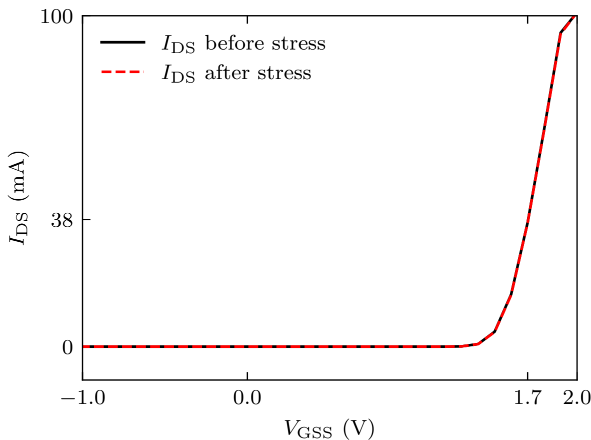
After determining the approximate 1-pulse BV_{dyn}, the gate of two p-GaN HEMTs GS-065-004-1-L were submitted to a series of three $15\,V$ OVS displayed in Fig. 9. The superposition of the three pulses show the excellent replicability of the stress.

To monitor the gate and its possible degradation, two indicators are used: gate leakage and gate threshold measurements. The corresponding measurements are respectively presented in Fig. 10a and Fig. 10b.

No degradation was detected in Fig. 10, thus showing the robustness of GaN HEMTs to at least few, short gate voltage OVS.



(a) Gate leakage monitoring, before and after stress.



(b) Gate threshold monitoring. The B1505 compliance was set to $100\,mA$.

Fig. 10: Degradation monitoring on the gate. The chosen health monitoring parameters show no sign of degradation.

This result and the measured 1-pulse BV_{dyn} are coherent with Wang et al. [2], although with different gate OVS waveforms. The switching energies are much lower with voltage OVS, as displayed in Fig. 8; this is related to the higher dV/dt with overshot waveforms, or the overshoot itself.

V. Conclusion

This work develops theoretical tools to apply any given voltage or current on a power device gate through ordinary $50\,\Omega$ cables. Similarly, the drain side circuit can be moved away (e.g. one meter).

As a demonstration, the spike breakdown voltage of a GaN gate was measured at four times the nominal gate voltage. A few stress waveforms as high as twice the DUT nominal rating have no measurable impact on the gate health.

This demonstration emphasizes the advantages of the setup: the interactions between the instrumentation circuitry and the DUT are suppressed, as well as parasitics.

Thus, this setup can be used for various testings, including long term gate reliability studies (e.g. repeated overshoots using realistic gate waveforms). Easier gate health monitoring is enabled, as well as gate signal optimization to achieve optimal switching in power converters.

Cable and tracks of any length can be used with the proposed setup. Especially, the use of long cables highly simplify environmental, thermal and wafer-level dynamic characterization.

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