# Assessing a precise gPTP simulator with IEEE802.1AS hardware measurements

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# Agenda

## Introduction

- Context
- IEEE 802.1AS
- Motivations

## Simulation

- Simulation library
- New inaccuracy sources

## Results

- Experimental protocol
- Calibration and validation

## Conclusion



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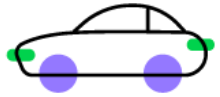
# Introduction – TSN

## EDEN : Evaluation of a Deterministic Ethernet Network

- Get full confidence and enable deployment of Ethernet Time Sensitive Network (TSN) as embedded network for multi domains architectures (aeronautic, automotive and spatial)

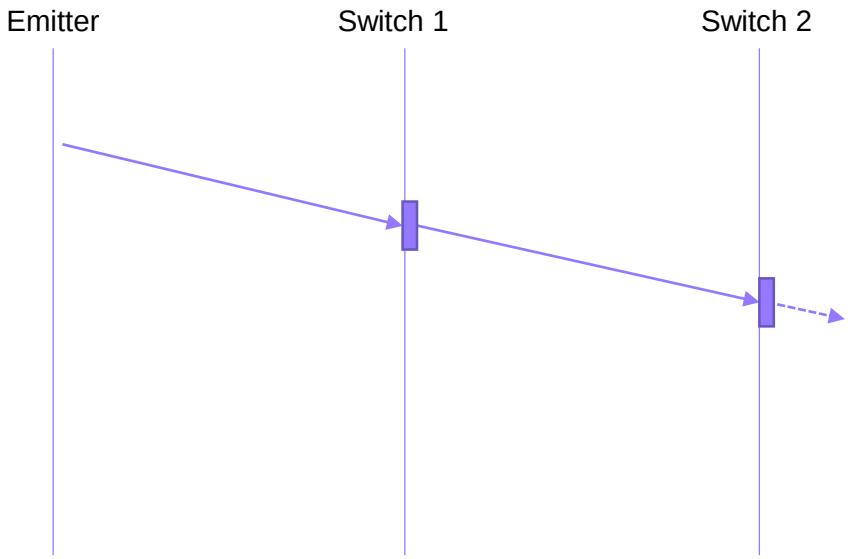

## TSN : Time-Sensitive Networking

- Aims to make classical Ethernet robust and deterministic
- IEEE Standard
- Some pros : unified network, large bandwidth choice, Ethernet ecosystem …

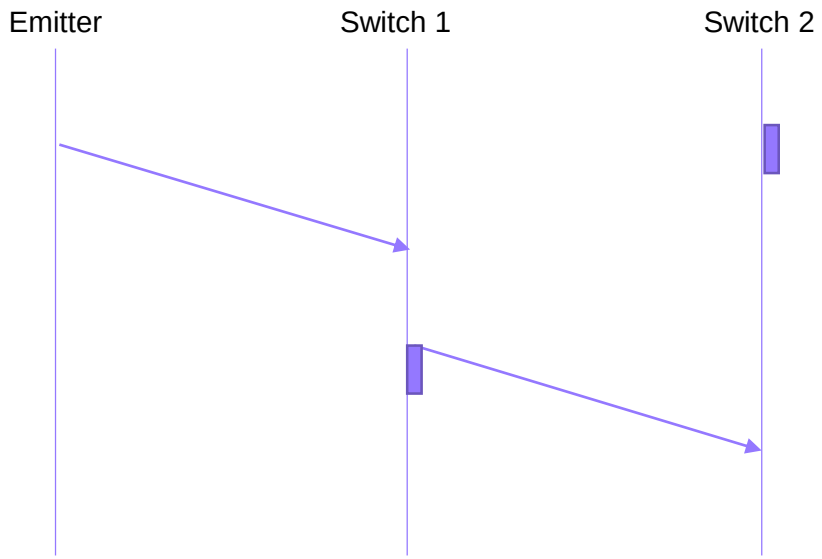
# Introduction – TAS

## Time Aware Shaper : Time bandwidth sharing

- IEEE802.1Qbv




A Time Aware Shaper example with synchronization.

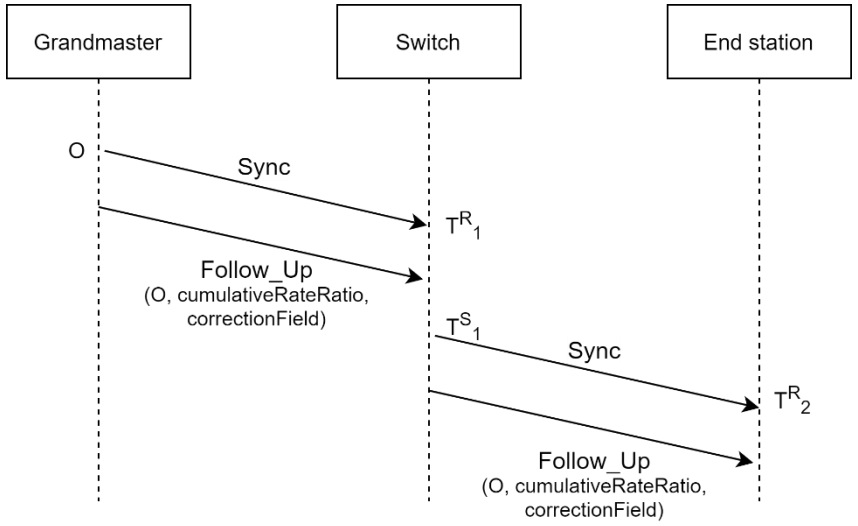



A Time Aware Shaper example without synchronization.

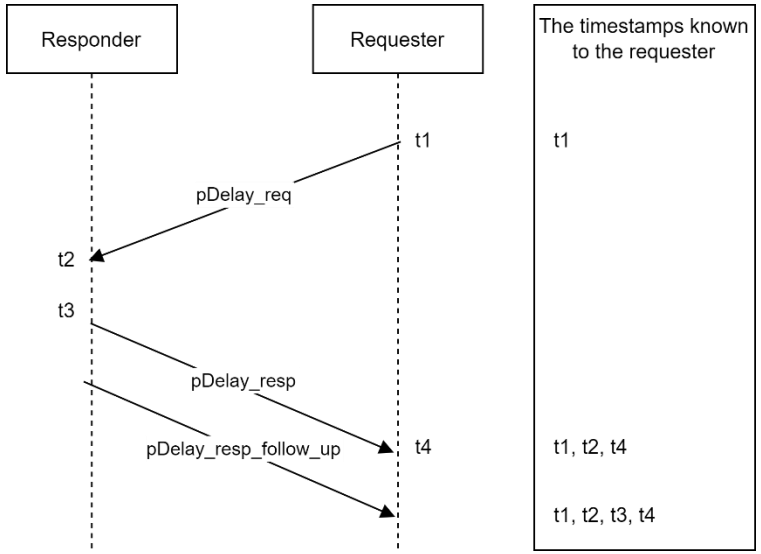
# Introduction – IEEE802.1AS

## IEEE802.1AS : gPTP, the TSN synchronization protocol

- A precise device called Grandmaster distribute periodically his clock to the network
- Based on PTP (IEEE1588)
- Precision goal : sub-microsecond in a 7-hop network
- For synchronization of embedded applications and time bandwidth sharing
- Distribution of synchronization messages from the Grandmaster to the time-aware systems
- Propagation delay measurement




Synchronization distribution mechanism.




Propagation delay measurement mechanism.

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# Introduction – Motivations

## **Simulation :** What precision can we achieve?

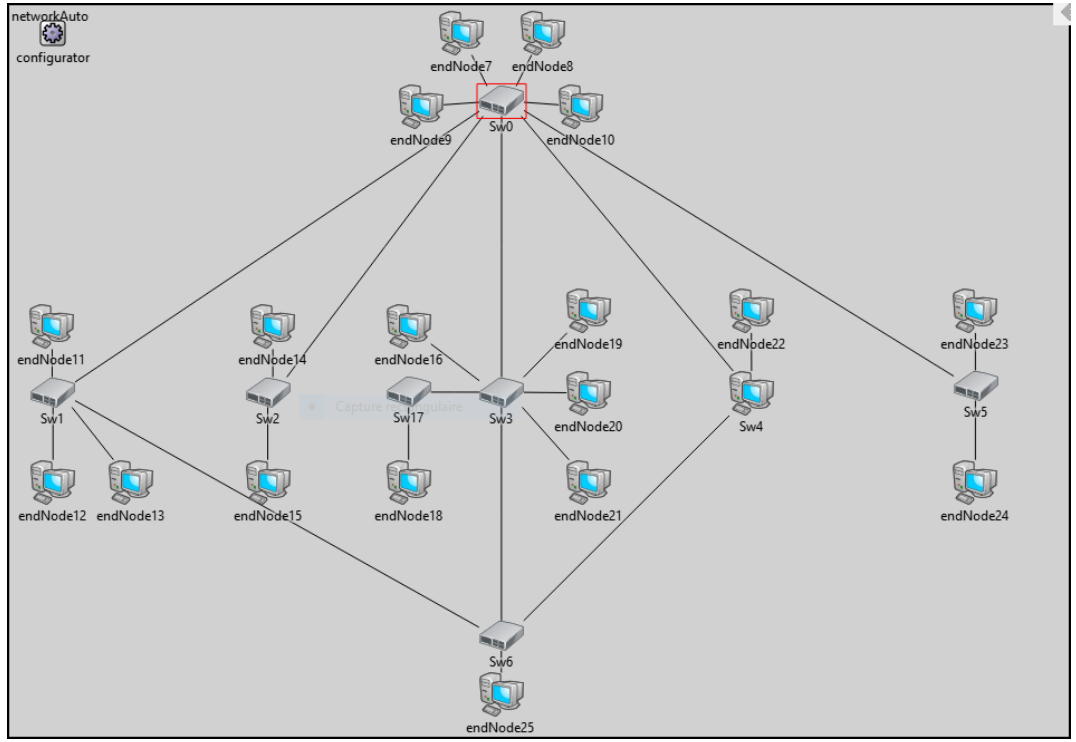
- Study of the average precision
- Experiment with new mechanisms  or configurations
  - Pdelay filter
  - Clock servo
  - Hot-standby
  - …

Is my IEEE802.1AS simulator representative of reality?

# Simulation

## **Simulation :** How to be representative of the reality ?

- Improvement of an open-source OMNeT++/INET library [1] :
  - Implementation a missing mechanism of the standard (logical syntonisation)
  - Addition of inaccuracy sources (For 100Base-T)
  - Minor bug fixes




Screenshot of one of a tested topologies with the simulator



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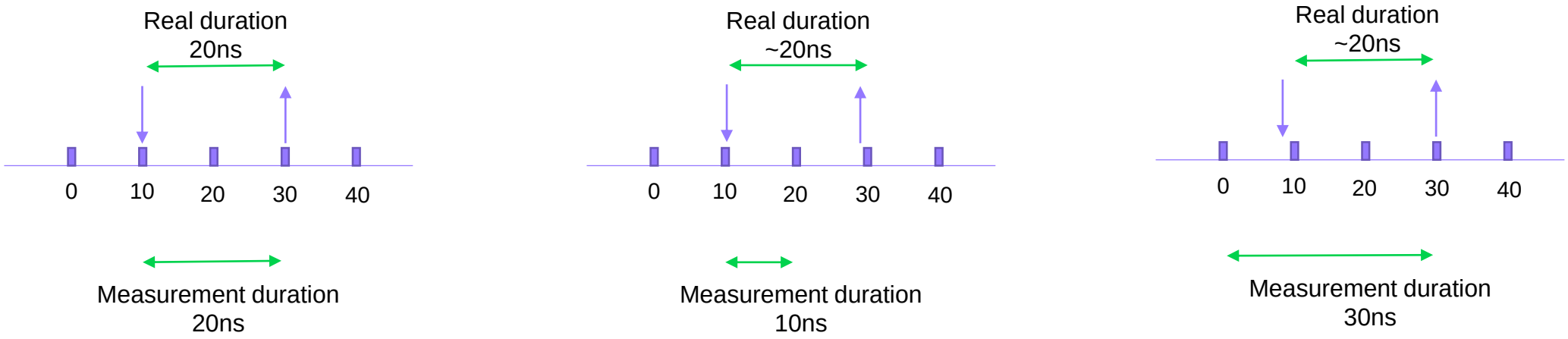
[1] : "A Simulation Model of IEEE 802.1AS gPTP for Clock Synchronization in OMNeT++", Henning Puttnies, Peter Danielis, Enkhtuvshin Janchivnyambuu, Dirk Timmermann, In Proceedings of the OMNeT++ Community Summit 2018, Vol. 56, pp. 63-72, Pisa, Italy, September 2018

# Simulation - Added inaccuracy sources

## Clock granularity :

- Quantization of time
- Error on every duration measurement
  - +/- the granularity

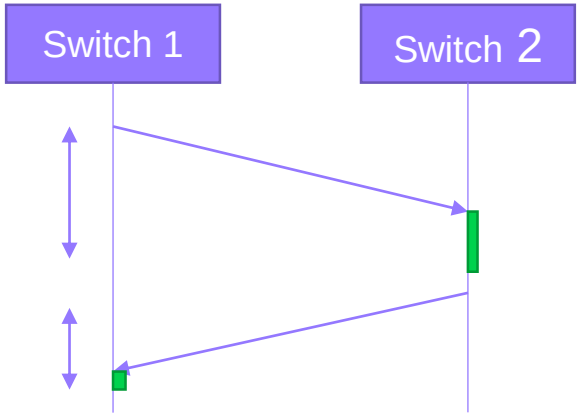



Example of the granularity (10ns) impact on duration measurement

# Simulation - Added inaccuracy sources

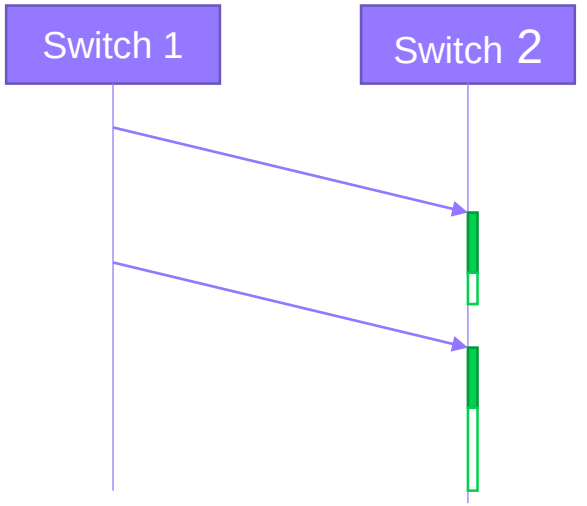
## Physical latency :

- After link establishment, constant 1-5 bit buffering (8-40 ns)
- Cause asymmetry in the propagation delay measurement mechanism




## Physical jitter :

- Variable processing delay in the physical layer
- Normal law



# Results – Experimental protocol

## **Clock simulation :** Constant drift or complex model ?

- Simple constant drift clock model calibration

## **Pdelay mechanism :** Calibration of the inaccuracy sources

- Calibration of the granularity
- Calibration of the physical inaccuracy sources

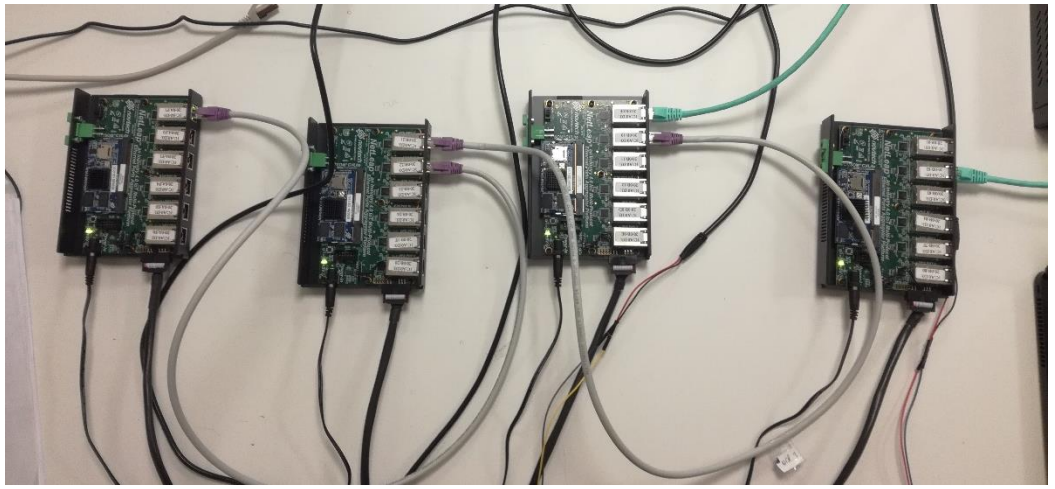
## **Synchronization :** validation of the representativeness

- Clock offset comparison between simulation and reality

# Results – Experimental topology

## Testbed presentation :

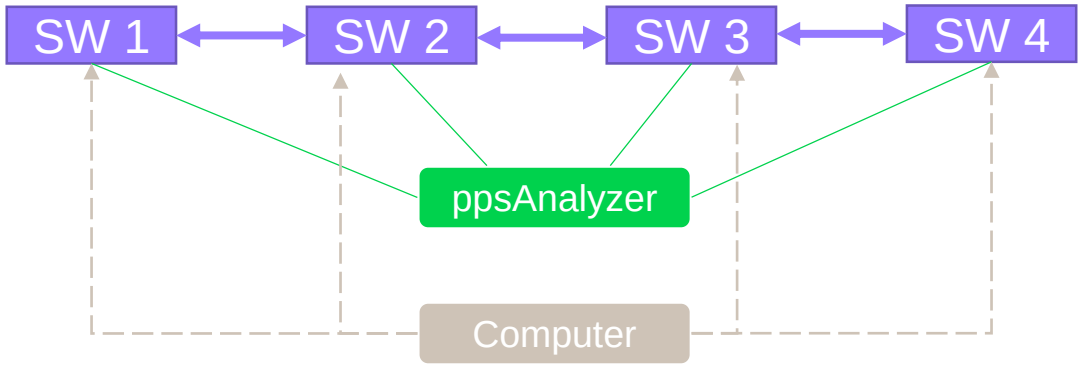
- 4 Fraunhofer IPMS TSN Switch
- netTimeLogic PPS analyzer



Picture of the network topology

## AS and simulation configuration :

- syncInterval : 0.125s
- pdelayInterval : 1s
- Clock drift : TBD
- Granularity : TBD
- Phy jitter : TBD




Experimental testbed

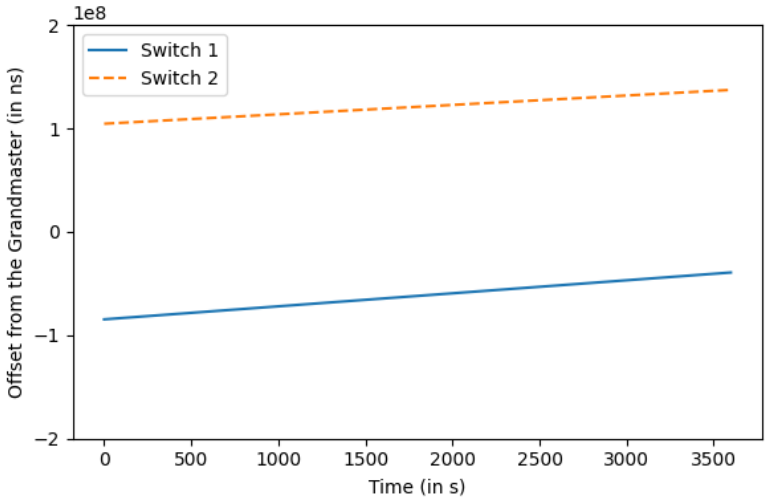
# Results – Clock calibration

**Clock simulation :** Do we need a complex model ?

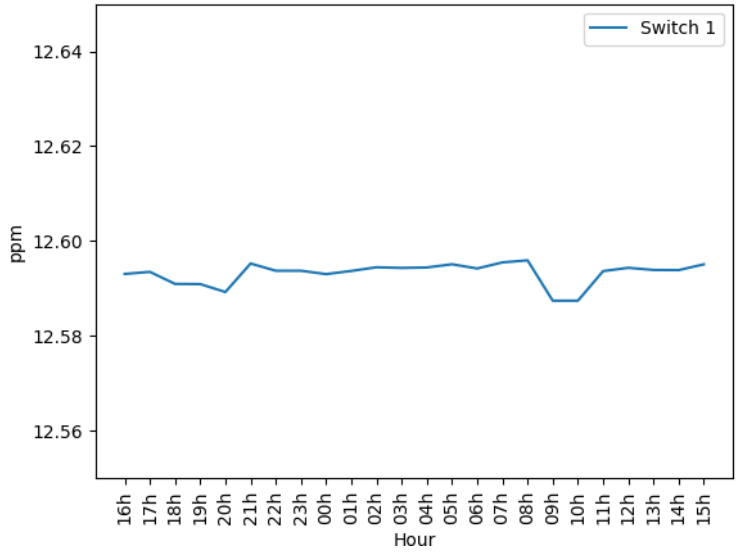
- Study of the clock drift in free running
- 24 1-hour experiments

➔ Linear behavior

- Clock drift rate from the slope
- Small variation during the day due to temperature variation (+/- 0.01ppm)




Grandmaster clock offset of two switches during 3600s




Clock drift rate variation during 24h

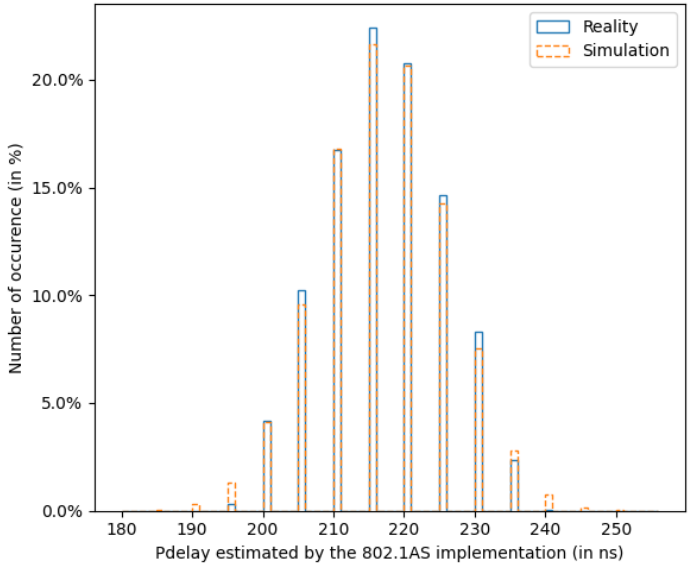
# Results – Pdelay mechanism

## **Pdelay mechanism :** Calibration of the inaccuracy sources

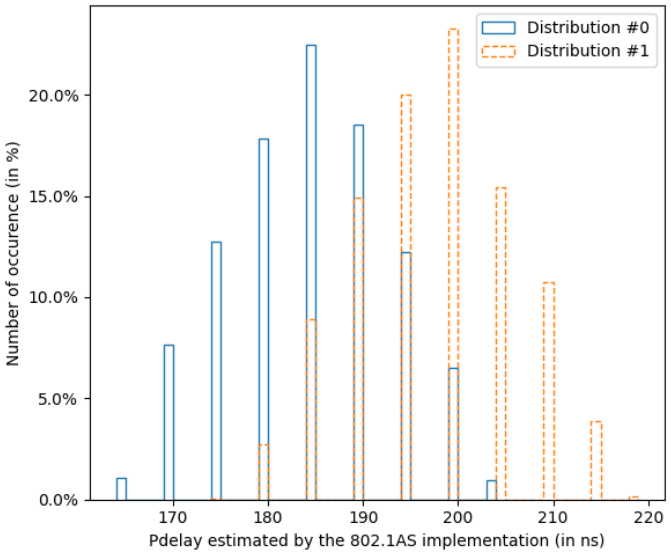
- Study of the distribution of the pdelay values between two switches

- Granularity = 10ns
  - From the separation between different pdelay values
- Phy jitter standard deviation = 12.5ns
  - From MSE minimization between simulated distribution and real distribution

➔ MSE < $10^{-5}$ between simulated and measured distribution after calibration




Comparison of simulated and measured Pdelay distribution after calibration




Comparison of two consecutive 1-hour Pdelay distribution

# Results – Synchronization

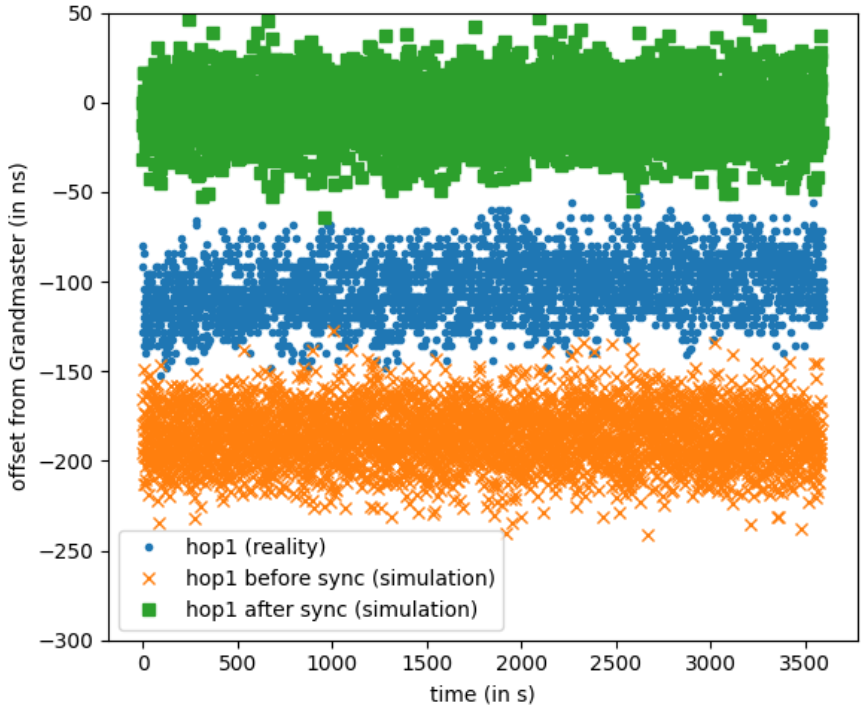
## Synchronization : validation of the representativeness

- Study of the clock offset between the Grandmaster and the other three node
- Simulation two bounds :
  - Just before synchronization (worst precision)
  - Just after synchronization (best precision)
- Reality :
  - 1 sample every second

➔ Simulator can bound the real precision

➔ Is our bounds accurate ?

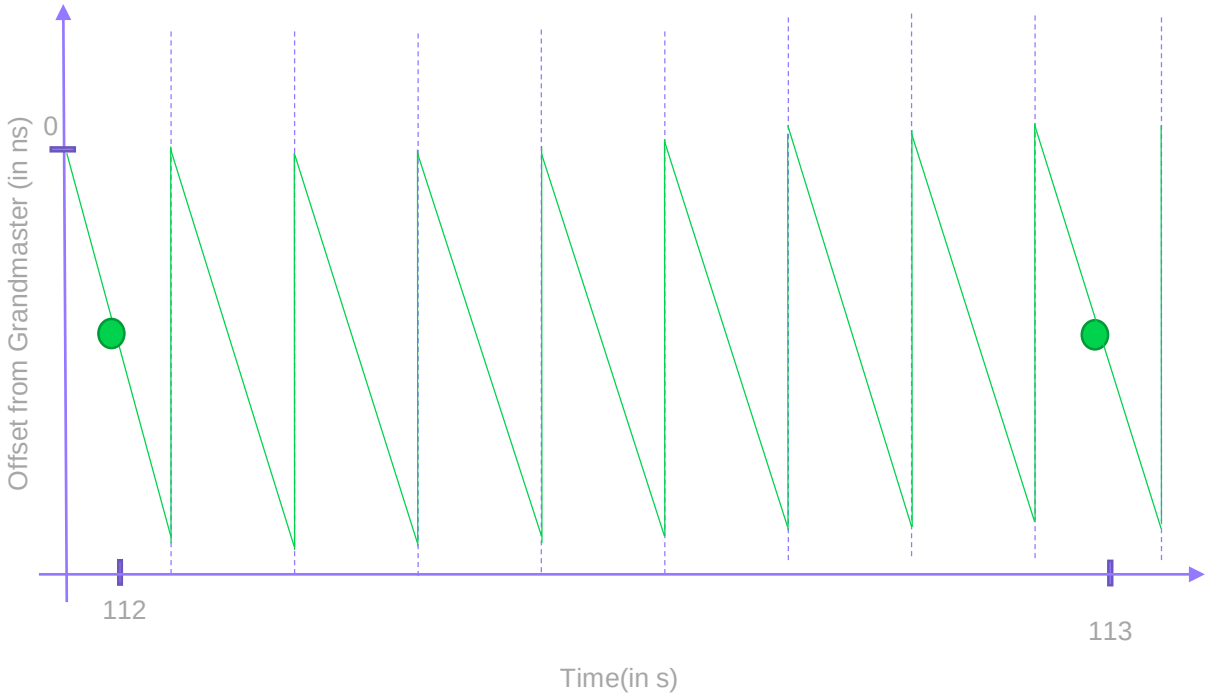
- We don't know when the PPS measurement is in the synchronization cycle.

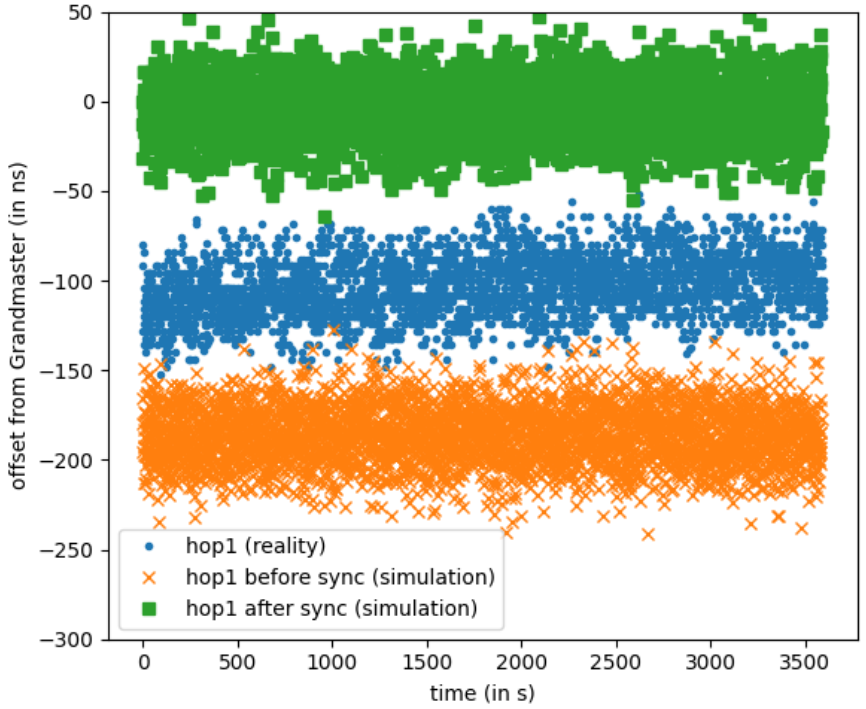



Offset between the Grandmaster clock and the switch clock at hop #1 in reality and the simulator.

The simulator is configured with the granularity and the standard deviation estimated in the previous experiments. For the clock drift, we use the drift measured before each experiment.

# Results – Synchronization

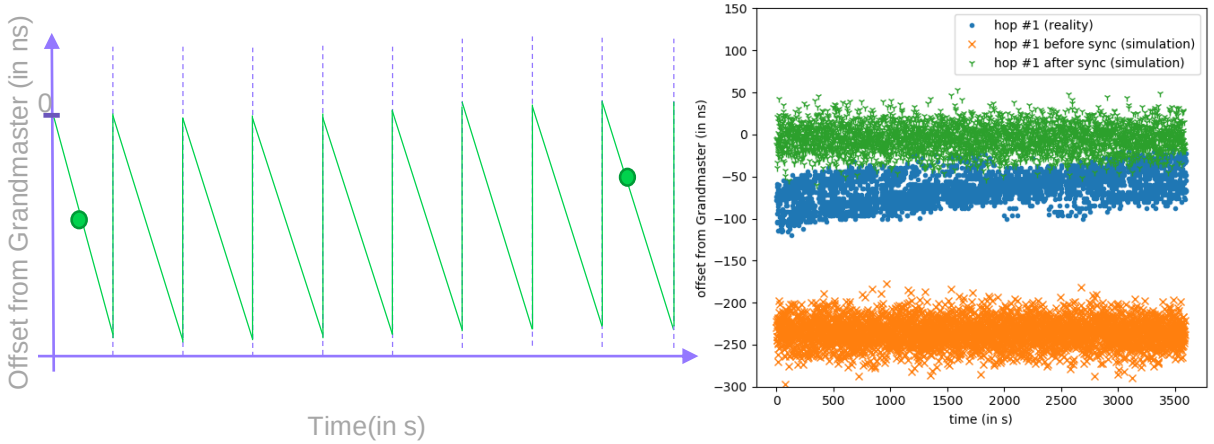


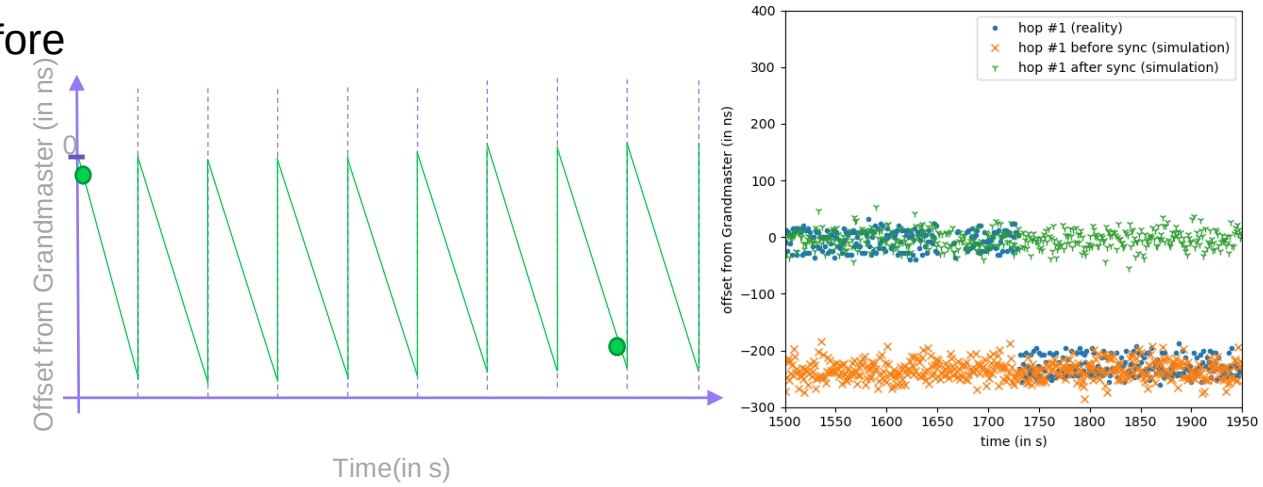
# Results – Synchronization

## Synchronization : PPS Gap

- Sync are not exactly send every 125ms
  - They are faster



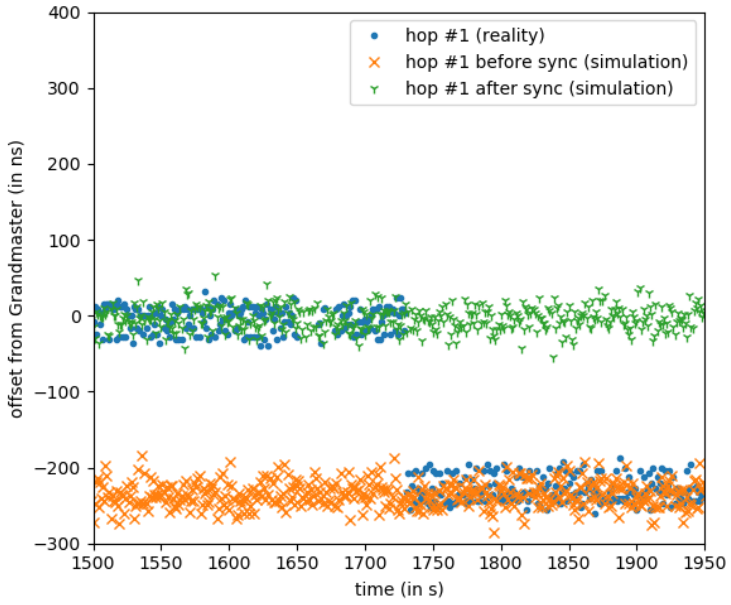

- When the whole second pass from before to after the synchronization:
  - PPS Gap
  - Position in the synchronization cycle



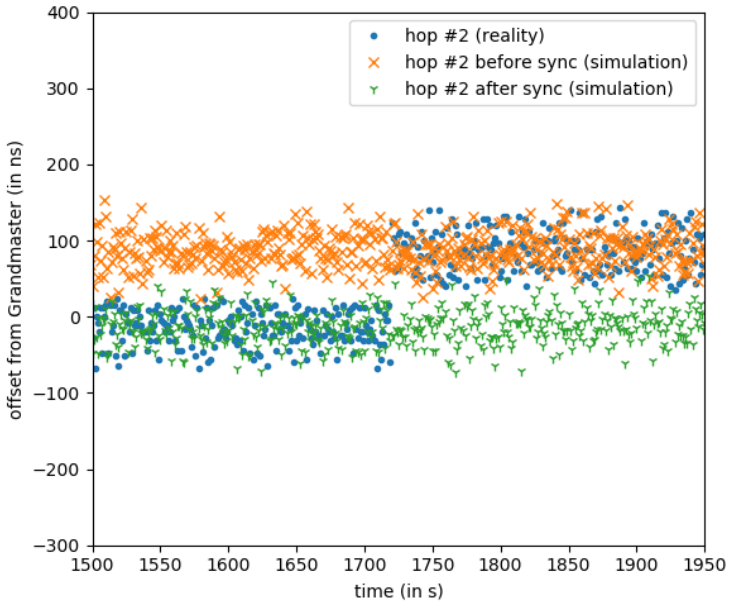
# Results – Synchronization

## Synchronization : PPS Gap

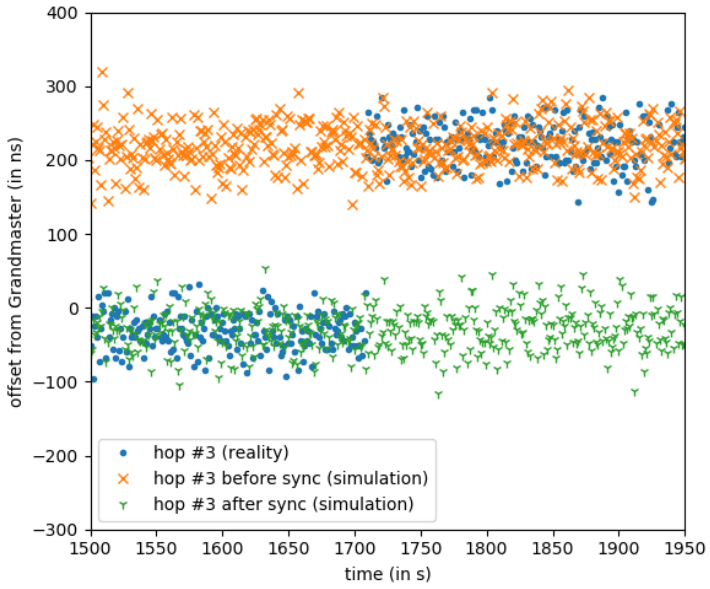
Offset from Grandmaster (in ns)




Hop #1




Hop #2




Hop #3

Offset between the Grandmaster clock and the switch clock in reality and the simulator with a PPS Gap.

# Conclusion

## A realistic open source simulator for IEEE802.1AS

- After calibration,  we got a RMSE of approximately 3 ns between sliding average of the precision measured and simulated.

## A three-step method to calibrate the simulator

- For different hardware
- For different physical layer

## Future work

- Worst-case precision

# Thank you for your attention

# Question ?

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