Three-dimensional vertical Si nanowire MOS capacitor model structure for the study of electrical versus geometrical Si nanowire characteristics

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Three-dimensional (3D) Si surface nanostructuring is interesting towards increasing the capacitance density of a metal-oxide-semiconductor (MOS) capacitor, while keeping reduced footprint for miniaturization. Si nanowires (SiNWs) can be used in this respect. With the aim of understanding the electrical versus geometrical characteristics of such capacitors, we fabricated and studied a MOS capacitor with highly ordered arrays of vertical Si nanowires of different lengths and thermal silicon oxide dielectric, in comparison to similar flat MOS capacitors. The high homogeneity and ordering of the SiNWs allowed the determination of the single SiNW capacitance and intrinsic series resistance, as well as other electrical characteristics (density of interface states, flat-band voltage and leakage current) in relation to the geometrical characteristics of the SiNWs. The SiNW capacitors demonstrated increased capacitance density compared to the flat case, while maintaining a cut-off frequency above 1 MHz, much higher than in other reports in the literature. Finally, our model system has been shown to constitute an excellent platform for the study of SiNW capacitors with either grown or deposited dielectrics, as for example high-k dielectrics for further increasing the capacitance density. This will be the subject of future work.

\textbf{1. Introduction}

Arrays of vertical Si nanowires (SiNWs) on a silicon substrate have attracted a lot of interest as a means of 3D nanostructuring towards increasing the effective capacitance area of a MOS capacitor compared to the flat Si case. Such capacitors find important applications as decoupling [1] and energy storage capacitors [2], including on-chip energy storage [3–6]. The explored 3D structuring and resulting increase in effective area and capacitance allows for a reduced device footprint, significantly reducing their cost.

Research efforts so far in the above direction have been concentrated on maximizing the capacitance density of the devices, while other important parameters were far from being optimized. For example, values of 18 μF/cm\textsuperscript{2} were reported in Ref. [3], 5.3 μF/cm\textsuperscript{2} in Ref. [4] and 2.6 μF/cm\textsuperscript{2} in Ref. [6], however the high capacitance has been achieved at the cost of reducing the maximum working frequency (cut-off frequency) and causing deviations of the measured capacitance from the designed values. For example, the cut-off frequency of the devices reported in Refs. [3–5] is only 1 kHz. This is due to the high series resistance in these devices, resulting from the reduced SiNW diameter, necessary to achieve maximum increase in the effective area of the capacitor [5]. Moreover, in Refs. [3,5] the SiNWs were grown by using bottom-up techniques [7,8], in which the density and position of the SiNWs was random and not exactly known, while there was large dispersion in their diameter and length. On the other hand, for the SiNWs in Ref. [4] the authors used metal-assisted chemical etching (MACE) [9–12], combined with lithographic patterning for the localization of the fabricated SiNWs. However, the above introduced an increased complexity of the fabrication, while the measured capacitance was still not in good agreement with the calculated one by considering the device effective surface area. In a recent publication by our group using SiNWs fabricated by MACE [6], a capacitance density of 4.1 μF/cm\textsuperscript{2} has been achieved, at a cut-off frequency above 1 MHz. This is a very good result, achieved by reducing the SiNW surface roughness through chemical treatment, and thus reducing density of interface states and leakage current. Another issue towards optimizing the capacitance density and cut-off frequency of the SiNW 3D capacitors is the difficulty in achieving good dielectric and metal coverage of the SiNWs.

In this work we present the fabrication and characterization of a SiNW MOS capacitor using a vertical SiNW array model structure. The crystalline SiNWs in the array were fabricated using a combination of I-line optical lithography and highly anisotropic reactive ion etching, allowing for a precise control of their location, diameter and height, and thus also their density. The diameter and interdistance of the
SiNWs were large enough so as to assure exact pattern transfer to the wafer and exact knowledge of SiNW number and density within the capacitor surface area. The characterization of the corresponding MIS capacitor allowed the extraction of different single SiNW parameters in a simple and accurate manner. The large diameter of the SiNWs allowed for a small series resistance and thus a cutoff frequency above 1 MHz for both dielectrics used.

2. Sample description

The Si wafers used were n-type with a resistivity of 1–2 Ω·cm. Arrays of SiNWs were formed on square areas covering the whole 4-inch wafer using a combination of photolithography and deep reactive ion etching. The fabrication process was described in detail elsewhere [13]. All process steps are compatible with standard Si processing. For the photolithography, an i-line stepper (FPA CANON 3000I4) has been used, with a critical resolution of 350 nm at wafer scale. The resist used was a 1.1 μm thick positive photoresist ECI from MICROCHEM CORP. For the Si etching an inductively-coupled plasma (ICP) reactor was used, with a critical resolution of 350 nm at wafer scale. The resist used was formed with a pitch of 1.1 μm. A square pattern of Si NWs was formed with a pitch of 1.1 μm. Two different SiNW lengths were examined, namely 1.35 μm and 2.5 μm.

Characteristic scanning electron microscopy (SEM) images at 45° angle of incidence of the 1.35 μm and 2.5 μm SiNWs are depicted in Fig. 1(a) and (b), respectively. Their surface is quite smooth and their diameter increases only slightly from their top to bottom. A top view SEM image at 45° angle incidence of the sample (c) and a SE micrograph (d) are depicted in the same figure. The large diameter of the SiNWs allowed for a simple and accurate manner. The large diameter of the SiNWs allowed for a small series resistance and thus a cutoff frequency above 1 MHz for both dielectrics used.

- Oxidation for the formation of the 6 nm thick SiO2 dielectric
- Phosphorus implantation and annealing for back ohmic contact formation
- Deposition and patterning of a 1 μm thick Al layer on the front surface area for contact and gate metal formation. The size of the contacts was 300 μm by 520 μm.
- Oxide removal from the back side, followed by 500 nm Al layer deposition and annealing for back ohmic contact formation
- Forming gas (mixture of H2/N2) annealing for interface trap minimization

In the case of the SiNW capacitor, the gate contact was taken outside the SiNW area in order to avoid their damage through probe contacting. The contact area was 300 μm × 100 μm and the SiNW area was 300 μm × 420 μm for the 1.35 μm SiNWs. For the 2.5 μm SiNWs the contact area was 520 μm × 100 μm and the SiNW area was 520 μm × 200 μm. Since no field oxide was used for defining the capacitor area, the contact area in the case of the SiNW capacitor was considered as a parallel flat capacitor and was taken into account in the calculations. The number of SiNWs in each SiNW capacitor was calculated with accuracy. A schematic representation of the fabricated capacitors is depicted in Fig. 1(d). Each sample had a surface area of 2 × 2 cm² and contained eight similar MIS capacitors, which were all measured.

3. Experimental results

Typical capacitance-voltage (C-V) characteristics of the three different measured devices (the flat capacitor and the SiNW capacitors with the two different NW lengths) are depicted in Fig. 2 for frequencies in the range 10³–10⁶ Hz. The different capacitor parameters are also depicted in the same figure. The flat-band voltage was determined at 1 MHz using the well-known method described in Ref. [14]. For the series resistance (Rs) and the oxide capacitance (Cox) we used the formulas [15]:

\[ R_s = \frac{G_{acc}}{G_{acc}^2 + \omega^2 C_{acc}^2} \]

\[ C_{ox} = C_{acc} \left[ 1 + \left( \frac{G_{acc}}{\omega C_{acc}} \right)^2 \right] \]

where \( \omega = 2\pi f \) and \( G_{acc} \) and \( C_{acc} \) are the values of conductance and capacitance at accumulation, respectively. Finally, the quality factor (Q) for the measured capacitors was calculated from:

\[ Q = \frac{f_{max}}{f_{ave}} \]

Fig. 1. SEM image at 45° angle incidence of the sample with Si NWs of (a) 1.35 μm and (b) 2.5 μm length and a 1.4 μm pitch. (c) Top view SEM image of the SiNWs, illustrating the SiNW diameter and pitch parameters. (d) Schematic representation of a flat and a MOS capacitor using the SiNWs.
The parameters extracted from the data in Fig. 2 for a frequency of 1 MHz are summarized in Table 1. The maximum deviation of the measured and extracted parameters is also indicated in the table. It is clear that this deviation is quite small, at least within the surface area of 2×2 cm² of the samples used. One can also see that the quality factor is well above 1 for all measured capacitors, which means that the cutoff frequency is well above 1 MHz and does not influence our results. The smaller quality factor of the SiNW capacitors compared to the flat ones is due to their much larger capacitance, since Q is inversely proportional to this capacitance. Moreover, the presence of the SiNWs does not significantly shift the flat-band voltage as compared to the flat case, revealing that the dielectric has comparable density of charged defects in all cases. The obtained capacitance and series resistance values will be further analyzed in the discussion section below.

The measured capacitance depicted in Fig. 2 was corrected for the parallel capacitance of the probe contact area by subtracting the flat capacitance for the corresponding contact area at a frequency of 1 MHz. The capacitance density as a function of applied voltage for all three measured devices at 1 MHz is depicted in Fig. 3, while the value of the capacitance density at accumulation in all three cases is given in Table 1. It can be seen that the capacitance density increase compared to the flat case is ×2 in the case of the 1.35 μm SiNWs, very close to the calculated ×1.9 by considering the surface area increase by the presence of the SiNWs. On the other hand, in the case of the 2.5 μm long SiNWs the corresponding factor is ×2.4, smaller than the calculated one (×2.7). A discussion on this discrepancy can be found in the following section.

The displacement current versus voltage of the three types of capacitors is given in Fig. 4(a), measured at a scan rate of 0.1 V/s for both positive scans (from −2 V to 2 V) and negative scans (from 2 V to −2 V). This displacement current results from the charging and discharging of the capacitors and can be expressed as:

\[ I = C \frac{dV}{dt} \]

From the displacement current characteristics we deduce the low
The low frequency capacitance versus voltage for all measured devices is depicted in Fig. 4(b). The corresponding 1 MHz curves for the flat and the 1.35 μm SiNW capacitors were also included for comparison, illustrating the good agreement between the low and high frequency curves at accumulation, as expected. This is another indication that the cutoff frequency of our NW capacitors is well above 1 MHz.

Deviation from the expected behavior is only found at accumulation and inversion regions of the 2.5 μm SiNWs. The displacement current increases rapidly in these regions, indicative of the presence of increased leakage current in this capacitor and the low frequency capacitance at deep inversion decreases abruptly. These will be further analyzed in the next section.

The leakage current versus voltage characteristics for all three devices are depicted in Fig. 5. The leakage current was measured at a scan rate of 0.01 V/s (an order of magnitude lower than the scan rate for the displacement current measurements). Scanning was performed from −2 V to positive 2 V in all cases. The leakage current at +2 V (accumulation) for each device is depicted in Table 1. Compared to the flat case it is increased by a factor of 5.9 in the case of the 1.35 μm SiNWs, while in the case of the 2.5 μm SiNWs this increase is ×162. This result will be discussed in detail below.

The density of interface states (Dit) has been calculated for the capacitors discussed above using the conductance method [14,15]. This method has been chosen since it is generally considered to be the most accurate down to densities of 10^9 states/V cm^2. The parallel conductance over angular frequency (Gp/ω) vs. angular frequency (ω) graphs for all three devices are presented in Fig. 6. From these curves we can calculate:

\[ D_{it} \approx \frac{2.5}{q A} \left( \frac{G_p}{\omega} \right)_{\max} \]

where \( q \) is the charge of the electron and \( A \) is the capacitor area.

From Fig. 6 it is clear that the corresponding values of \( D_{it} \) for all
three capacitors are in all cases only 2 to $5 \times 10^{10} \text{states/V-cm}^2$, which is an indication of the good electronic quality of the SiO$_2$/Si interface. This is attributed to the smooth SiNW surface and the absence of any contamination during processing. The $D_{n}$ of all measured devices are also depicted in Table 1.

4. Discussion

In order to better understand the results presented in the previous section we calculate the expected capacitance for each measured devices by taking into account the capacitor surface area. So, for the flat capacitor we have:

$$C_{\text{flat}} = \frac{\varepsilon_0 A}{d} = 8.9 \times 10^{-10} \text{F}$$

where A is the capacitor surface area, namely 300 $\mu$m by 520 $\mu$m, d is the dielectric thickness (6 nm), $\varepsilon$ is the dielectric constant of SiO$_2$ (3.9) and $\varepsilon_0$ is the vacuum permittivity.

In the case of the SiNW capacitors, the total capacitance is the sum of the capacitance of the flat surface area plus the capacitance of a single nanowire multiplied by the total number of SiNWs. The single SiNW capacitance can be calculated using the cylindrical capacitance relationship:

$$C_{\text{NW,single}} = \frac{2\pi \varepsilon_0 h}{\ln\left(\frac{r + h}{r}\right)}$$

where h and r are the height and radius of each SiNW respectively. So, for $h_1 = 1.35 \mu$m and $h_2 = 2.5 \mu$m we have:

$$C_{\text{NW,single1}} = 1.3 \times 10^{-14} \text{F}$$
$$C_{\text{NW,single2}} = 2.4 \times 10^{-14} \text{F}$$

The total SiNW capacitance for the two different SiNW lengths is:

$$C_{\text{NW, total1}} = N_1 \times C_{\text{NW,single1}} = 8.2 \times 10^{-10} \text{F}$$
$$C_{\text{NW, total2}} = N_2 \times C_{\text{NW,single2}} = 1.25 \times 10^{-9} \text{F}$$

where N$_1$ and N$_2$ is respectively the number of SiNWs in each case.

The calculated total capacitance of each SiNW capacitor is respectively:

$$C_{\text{total1}} = C_{\text{NW, total1}} + C_{\text{flat}} = 1.7 \times 10^{-9} \text{F}$$
$$C_{\text{total2}} = C_{\text{NW, total2}} + C_{\text{flat}} = 2.1 \times 10^{-9} \text{F}$$

These values are depicted in Table 1 as the calculated values of capacitance. It can be easily seen that they coincide nicely well with the measured values in the cases of the flat and 1.3 $\mu$m SiNW capacitors, while a small deviation (approximately 15%) exists in the case of the 2.5 $\mu$m SiNWs. One possible explanation for this deviation is the increased leakage current at accumulation and inversion regions in the case of the 2.5 $\mu$m SiNWs, depicted in Fig. 5(b) and the corresponding value at 2 V given in Table 1. It can be seen that the leakage current does not scale with the increase in the capacitor area (close to a factor of 2 in both SiNW cases compared to the flat devices), but by a factor of 5.9 compared to the flat in the case of the 1.35 $\mu$m SiNWs and a factor of 162 in the case of the 2.5 $\mu$m ones. Clearly, the leakage current increase in the case of the 1.35 $\mu$m SiNWs is moderate, while it is very large in the case of the 2.5 $\mu$m SiNWs case, which explains the observed deviation in the low frequency capacitance measurements and possibly the 15% deviation in the high frequency measurements. The increased leakage current in the case of the SiNW capacitors beyond what is expected by the increase in effective area is attributed to increased roughness at the SiNW vertical surfaces compared to the flat case, resulting from the etching process. Additionally, the existence of corners in the SiNW 3D structure is at the origin of dielectric thickness inhomogeneities and increased local electric fields, which are an additional source of leakage current. The above effects are more pronounced in the case of the longer SiNWs.

Another interesting observation is that the series resistance ($R_s$) is 38 $\Omega$ in the case of the flat capacitor, while it is 41 $\Omega$ and 44 $\Omega$ respectively in the cases of the shorter and longer SiNWs. The increased series resistance in the case of the SiNW capacitors (3 $\Omega$ and 6 $\Omega$ respectively) is attributed to the SiNW resistance, being larger in the case of the longer SiNWs. Indeed, the SiNW resistance for the two different nanowire lengths ($R_1$ and $R_2$) can be calculated as:

$$R_1 = N_1 \rho_0 \frac{h_1}{A'}$$
$$R_2 = N_2 \rho_0 \frac{h_2}{A'}$$

where $\rho_0$ is the resistivity of the Si wafer used, N is the number of SiNWs in the capacitor area, $l_1$ and $l_2$ is respectively the length of the SiNWs in each case and $A'$ is the cross sectional area of the SiNWs, which is considered to be the same in both cases. By setting the values of $R_1 = 3 \Omega$ and $R_2 = 6 \Omega$, the resulting wafer resistivity is found to be 2 $\Omega$cm and 1.85 $\Omega$cm respectively. These values are within the resistivity range of the substrates used ($1$–$2 \Omega$cm). As before, these measurements and calculations are possible in our model system because of the relatively small number and ordering of the SiNWs used.

The exact knowledge of the series resistance introduced by the SiNWs is very important since it is related to the capacitor cutoff frequency ($1/RSC_{ox}$) or the quality factor at a given frequency of a capacitor with a given capacitance value.

Based on the above, we have to conclude that the very good agreement between calculated and measured values of capacitance and series resistance, as well as the exact correlation of the electrical with structural properties of the SiNWs, has been made possible because of our model SiNW system. The large spacing between SiNWs and the conformal metal coverage allowed their use as a platform to investigate SiNW-based MOS capacitor properties and correlate to a single SiNW MOS capacitor characteristics.

5. Conclusions

In conclusion, we have developed and characterized SiNW MOS capacitors based on a model system of ordered arrays of vertical Si nanowires. Due to their large diameter and interdistance no proximity effects were present. This, along with an excellent size, shape and position of the SiNWs allowed to extract the capacitance density increase per SiNW. A measured capacitance density of 1.4 $\mu$F/cm$^2$ has been demonstrated for the fabricated capacitors, with cutoff frequency above 1 MHz, much higher than in other reports in the literature. The measured capacitance and series resistance were very close to the calculated ones by considering the geometrical characteristics of the model SiNW system. Finally, our model system is excellent for the study of SiNW capacitors with deposited dielectrics, as for example high-k atomic-layer deposited (ALD) dielectrics. This will be the subject of future work.

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References


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