High Performance CMOS FDSOI Devices activated at Low Temperature

L. Pasini1,2, P. Batude1, J. Lacord1, M. Casse1, B. Mathieu1, B. Sklenard1, F. Piegas Luce1, J. Micout1,2, A. Payet1, F. Mazen1, P. Besson1, E. Ghezin1,2, J. Borrel1,2, R. Dubriac1, L. Hutin1, D. Blachier1, D. Barge1, S. Chhun1, V. Mazzacchi1, A. Cros1, J-P. Barnes1, Z. Saghi1, V. Delaye1, N. Rambal1, V. Lapras1, J. Mazourier1, O. Weber1, F. Andreu1, L. Brunet1, C. Fenouillet-Beranger1, Q. Rahay1, G. Ghibaudo1, F. Cristiano1, M. Haond1, F. Bouet1 and M. Vinel1

CEA- Leti, Minatec Grenoble, 3STMicroelectronics Crolles, 1IMEP-LAHIC, Minatec Grenoble INP, 2LAAS-CNRS, Toulouse FRANCE

Abstract- 3D sequential integration requires top FETs processed with a low thermal budget (500-600°C). In this work, high performance low temperature FDSOI devices are obtained thanks to the adapted extension first architecture and the introduction of mobility boosters (pMOS: SiGe 27% channel / SiGe:B 35% RSD and nMOS: SiC:P RSD). This first demonstration of n and p extension first FDSOI devices shows that low temperature activated device can match the performance of a device with state-of-the-art high temperature process (above 1000°C).

I-INTRODUCTION:

Low Temperature (LT) devices can be stacked on other devices opening the path to extremely dense 3D sequential architectures with 3D connections up to 10² via/mm [1,2]. Recently, extension first (X¹st) architecture was identified as a potential solution to high performance low temperature activated devices [3]. In this work, LT X¹st integration and High Temperature (HT) Process Of Reference (POR) FDSOI devices are compared (flows in Fig.1). Channels (Si and 6nm thick SiGe 27% films on 20nm Buried Oxide (BOX)) and gate stack are similar (TINV=12.5Å and 14Å for n/pFDSOI respectively) for the two devices. In the LT flow, LDD implantations are done during the spacer etching process while in the HT a thin silicon liner is used. This enables to compensate for the lack of dopants diffusion from the in-situ doped RSD to LT compared to HT POR [3]. After the LDD implant, a nitride deposition complement is performed in order to drive the dopants from the in-situ doped RSD to the channel [4]. Note that, apart from its adaptation to LT device process, the X¹st flow offers better junction definition only by the thin liner thickness while in the HT POR flow the junction alignment depends on the i) spacer deposition thickness ii) spacer etching process iii) dopants diffusion. In this paper, the access resistance (RACCESS) will be decomposed in RCOFB/RSPA corresponding to the regions identified in Fig.2a.

II-RESULTS:

The technological challenges of X¹st integration are: i) the control of a thin amorphization thickness to obtain high activation level with LT Solid Phase Epitaxy (SPE) at 630°C requiring a partial film amorphization. Spacer etching is followed (in both LT and POR processes) by in-situ doped epitaxy: SiC:P and SiGe:B for the n/pFETs respectively. POR devices are submitted to a HT anneal to drive the dopants from the in-situ doped RSD to the channel [4]. Note that, apart from its adaptation to LT device process, the X¹st flow offers better junction definition only by the thin liner thickness while in the HT POR flow the junction alignment depends on the i) spacer deposition thickness ii) spacer etching process iii) dopants diffusion. In this paper, the access resistance (RACCESS) will be decomposed in RCOFB/RSPA corresponding to the regions identified in Fig.2a.

FDSOI devices were fabricated with the flow described in Fig.1a&b. The split table includes variations in Ge Pre-Amorphization Implanted (PAI) dose leading to different amorphization depths (Table 1). The No Implant splits present a dramatic performance decrease in both LT and HT POR (ΔRSP=80Ωxµm) while the nMOS (ΔRSP=80Ωxµm) shows slight room for improvement. This work provides some valuable insights on several critical integration aspects, and guidelines for further performance improvements are identified in the following sections.

RPF1 contribution: epitaxial regrowth quality degradation for the high P implant is evidenced by the epitaxy thickness, the ellipsometry Goodness Of Fit values (Fig.10) and the RSPET measurements for both n/p accesses (Fig.11). This degradation is not attributed to crystalline seed defectivity as it is also observed on bulk structures. All other splits present perfect epitaxial quality.

RSPET contribution: activation level of LT X¹st integration first FDSOI devices is different with or without HT anneal (6x10¹⁷ and 2x10¹⁰/cm² respectively) leading to RSPET degradation for LT splits compared to POR (Fig.11). To evaluate its impact on RSPET, No Implant and SiGe:B on-top LT POR (ΔRSP=80Ωxµm) was evaluated for both LT and HT splits leading to ARSP_LT-HT<0.8Ωxµm while the nMOS (ARSP_LT-HT<80Ωxµm) shows slight room for improvement. This work demonstrates record performance for low temperature activated devices with 800 and 630µA/µm ION at 100nA/µm and VDS=0.8V for n/p devices respectively. The X¹st integration, initially suited for LT activated devices has been demonstrated for the first time for both n/pFETs. Its challenges i.e. the controlled amorphization in a 6nm film and the epitaxy regrowth on implanted films are successfully overcome. Guidelines for further performance improvements are also identified. Besides the interest for 3D sequential integration, the architecture also offers opportunities to increase the junction position variation which only depends on the LT liner thickness deposited.

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Fig. 1: a) LT \(X^{14}\) integration process flow. Implantation through thin liner enables to place dopants at the channel entrance b) HT POR process flow. Dopants are activated by HT thermal anneal and driven by diffusion in the region below the spacer.

Fig. 2: a) \(R_{\text{ACCESS}}\) main contributions: NiPt/Si contact resistance \(R_{\text{C}}\), epitaxial region \(R_{\text{E}}\), region below the spacer \(R_{\text{SPA}}\). b) Devices split table.

Fig. 3: TEM micrograph showing partial amorphization of the thin SiGe film. a) Active B concentration profile (EVA) obtained after 630°C annealing compared to total B. An activation level of \(3 \times 10^{19}\) at/cm\(^2\) is achieved.

Fig. 4: \(R_{\text{SHEET}}\) mapping on 300nm wafer of an 6nm SiGe film activated by SPE at 630°C. b) Thickness mapping of the thin SiN liner used to define the junction position in the X\(^{14}\) integration on 300nm wafer (\(\Delta_{L}\) less than 1Å).

Fig. 5: TEM micrographs of n & pMOS Medium PAI splits transistors fabricated with LT \(X^{14}\) process. Good epitaxial growth quality on the implanted region is observed.

Fig. 6: nMOS \(I_{\text{OFF}}\)-\(I_{\text{ON}}\) trade-off for low temperature extension first devices compared to high temperature process of reference.

Fig. 7: pMOS \(I_{\text{OFF}}\)-\(I_{\text{ON}}\) trade-off for low temperature extension first device compared to high temperature process of reference.

Fig. 8: \(I_{\text{OFF}}\)-\(I_{\text{ON}}\) performance benchmark of LT FD-SOI devices for a) pMOS b) nMOS. nMOS HT \(X^{14}\) is also shown. These devices outperform both TriGate not shown here (\(\delta_{\text{LT}}\))

Fig. 9: nMOS \(R_{\text{ACCESS}}\) extraction with Y function method. The \(I_{\text{OFF}}\)-\(I_{\text{ON}}\) trade-off split evolution is explained by the \(R_{\text{ACCESS}}\) evolution.

Fig. 10: Epitaxy thickness and Goodness Of Fit (GOF) of the in-situ doped epitaxy regrowth on the implanted thin accesses. A clear degradation is observed for the High PAI splits in the the nMOS cases.

Fig. 11: nMOS \(R_{\text{SHEET}}\) measurements on regions with epitaxy regrowth on implanted films for SOI and bulk structures. High PAI \(R_{\text{SHEET}}\) indicates bad epitaxy quality. N LT \(R_{\text{SHEET}}\) indicates worse P activation in SiC:P if no HT anneal is performed.

Fig. 12: a) NiPt/n-Si contact resistivity extraction versus doping level taking into account FE, TE and TFE mechanisms. b) NiPt / n-Si contact resistance \(R_{\text{C}}\) extraction in the FD-SOI device versus doping level by full TCAD SDEVICE simulation.

Fig. 13: \(R_{\text{SHEET}}\) measurements on a 6 nm Si film implanted with the conditions reported in Fig.2b. Expected evolution is observed for the pFET case, i.e. \(R_{\text{SHEET}}\) decreases with the amorphization depth. For n-type the values are not consistent with usual SPE activation levels.

Fig. 14: a) Simulated N profile on the 6nm Si film with high PAI and No PAI n-type implants. High PAI split shows a clear increase of the nitrogen recoil concentration. b) Experimental SIMS measurement confirms the results in terms of count.

Fig. 15: \(R_{\text{OFF}}\) extraction by full FD-SOI device TCAD simulation (SDEVICE) as a function of the spacer thickness for various \(R_{\text{SHEET}}\) values. For both nMOS, the \(\Delta R_{\text{SHEE}}\) and \(\Delta R_{\text{OFF}}\) are consistent with the measured \(R_{\text{ACCESS}}\) difference between LT and POR splits.

Fig. 16: Pelgrorn plot of No PAI splits compared to the POR (nFET). Very good mismatch in line with data in literature [16] for both devices are shown.