Verification of Near-Interface Traps Models by Electrical Measurements on 4H-SiC n-channel MOSFETs

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\textbf{Keywords:} 4H-SiC MOSFETs, SiC/SiO\textsubscript{2} interface, NIT, donor and acceptor types of traps.

\textbf{Abstract.} 4H-SiC n-channel lateral MOSFETs were manufactured and characterized electrically by current-voltage measurements and by numerical simulation. To describe the observed electrical characteristics of the SiC MOSFETs, Near-Interface Traps (NIT) and mobility degradation models were included in the simulation. The main finding of the simulation is that two models for the NIT states in the upper part of the SiC bandgap are able to describe the electrical data equally well. In one of them, acceptor-like traps and fixed charge are considered while in a newly developed one, donor-like traps are taken into account also.

\textbf{Introduction}

SiC is a wide bandgap semiconductor with favorable physical properties [1] making it attractive for various applications in electronic industry. Its wide bandgap makes it ideal for operation in high temperature environments. The high thermal conductivity and high breakdown field make it the material of choice for high power MOSFETs. In addition, the possibility to form an SiO\textsubscript{2} layer on SiC by thermal oxidation in a way similar to Si provides a good basis for the fabrication of SiC-MOS-based electronic devices. Among the various polytypes of SiC, 4H-SiC is considered the most promising one for MOSFET development due to its high intrinsic carrier mobility. Unfortunately, commercial use of 4H-SiC MOSFETs is still limited by technological problems resulting in a low on-state current and a low inversion-layer electron mobility. The low performance of SiC-based MOSFETs is usually explained by the high concentration of Near-Interface Traps (NIT), leading to charge trapping and Coulomb scattering at the interface.

In this work, for the description of the electrical characteristics of the SiC MOSFETs, NIT and charge carrier mobility degradation models were included in simulations performed with the Sentaurus TCAD software. The essential finding of the comparison between simulations and measurements is that two of the models of NIT states in the upper part of the SiC bandgap are able to reproduce the experiments: A conventional model with only fixed charge and acceptor type states, and a new model that includes fixed charge and both the conventional acceptor type electron trap states and additional donor type energetic traps with a level near the conduction band of 4H-SiC. The aim of this paper is to analyze these two types of models and to verify their applicability by electrical measurements on 4H-SiC n-channel MOSFETs.

\textbf{Experiments}

In this study, n-channel lateral MOSFETs have been fabricated on a p-type 4°-off 4H-SiC (0001) Si-face epitaxial layer with an aluminum concentration of $5 \times 10^{17}$ cm\textsuperscript{-3}. A 34 nm thick gate oxide was grown by thermal oxidation in N\textsubscript{2}O atmosphere at 1553 K and annealed at the same temperature for 30 min under N\textsubscript{2} ambient. Phosphorus-doped polycrystalline silicon was deposited and patterned to form the gate electrode. Source and drain regions were box implanted with...
nitrogen with a peak concentration of $5 \times 10^{19}$ cm$^{-3}$. For the fabrication of the source and drain contacts, SiC was alloyed with titanium at 1373 K for 2 min and, thereafter, a metallization stack containing titanium and platinum was deposited and patterned. The channel length and width of the transistor are 500 µm and 80 µm, respectively. To characterize the MOSFETs electrically, current-voltage measurements were performed for different values of drain-source voltages (0.1 V, 0.6 V, 1.1 V). The gate voltages were swept from 0 V to 18 V in the measurements of the transistor transfer characteristics.

Results and discussions

Default simulations. One of the main tasks for numerical simulation is to explain the physical background for the low performance of the MOS transistors based on 4H-SiC with gate oxides produced by thermal oxidation. First, for reference, electrical properties of n-channel transistors were computed using the default model that assumes an ideal interface between the gate oxide and the 4H-SiC semiconductor in the channel. This assumption means that any fixed electrical charge at the gate-oxide-to-SiC interface is neglected and no interface trap charges are accounted for. The result of such a simulation for the SiC-MOSFET, described in the previous section, is shown in Fig.1 in comparison with the results of the measurements.

As expected, the simulation with an ideal interface between the gate oxide and the semiconductor is insufficient and deviates from measurements significantly. The ideal SiC MOSFET, according to simulation, has a higher than measured threshold voltage and a significantly, i.e. about a factor of 60, higher current compared to the one measured. The result indicates the necessity to include additional models into the simulation that will be able to describe SiC-specific physical phenomena in MOSFETs for achieving better agreement with experiments. Following the existing knowledge about the SiC/SiO$_2$ interfaces [1-4], we included in the simulation NIT and mobility degradation models due to Coulomb and surface roughness scattering mechanisms with the model parameters at which the best agreement with experiments was achieved.

Conventional NIT model. According to literature [2,3], there are two main classes of defects which contribute to the distribution of the interface trap density of states ($D_{it}$) across the SiC bandgap. A first class of defects spans the entire SiC bandgap with a density not exceeding $10^{12}$ cm$^{-2}$eV$^{-1}$. A second class of defects consists of electron traps in the upper half of the bandgap giving rise to a peak reaching $10^{13}$ cm$^{-2}$eV$^{-1}$ near the 4H-SiC conduction band. The defects responsible for the high $D_{it}$ close to the conduction band, considered as Near-Interface Traps, remain so far not well understood. We associate these traps to specific defects in the oxide, which introduce levels into the semiconductor bandgap. For the n-channel transistors considered in this work, NIT with energetic states close to the conduction band of SiC are of the most relevance. For the simulation of the interface trap density in the upper part of SiC bandgap as a function of the trap energy $E_t$, usually the conventional model from literature [1,4] is used and can be described as:

$$D_{it}(E_t) = D_{it}^{mld} + D_{it}^{edge} e^{\frac{E_t-E_c}{\sigma}} \quad \text{for } E_t \leq E_{peak}.$$  

The first component of the electronic states, $D_{it}^{mld}$, has a constant density over energy and dominates the energy state density near the middle of the bandgap. The other component, $D_{it}^{edge}$, is the band-edge density of states. It is modeled by an exponentially distributed tail characterized by the parameter $\sigma$ and has its maximum at $E_{peak}$ near the conduction band edge $E_c$. 

![Fig.1. Comparison of ideal simulations (lines) and measurements (symbols).](image-url)
It seems important to clarify here that the conventional NIT model assumes only acceptor-like states in the upper half of the SiC bandgap [1,2]. Traps are considered to behave similarly to doping impurities: An interface trap is considered donor-like if it is neutral and can become positively charged by donating an electron. An acceptor-like interface trap is neutral and becomes negatively charged by accepting an electron. The acceptor type states are able to trap electrons from the inversion layer, thus making them immobile and excluding them from participating in the electronic transport in the transistor channel. In this manner, acceptor traps can reduce the MOSFET current and enlarge the threshold voltage in comparison with the ideal MOSFETs behavior without any traps. In Fig. 1, we observe the opposite case. The experimental threshold voltage is lower than that predicted by the simulation for an ideal MOSFET without any interface states. Such a low threshold voltage as it is seen experimentally can only be explained either by the presence of a large positive fixed charge at the gate-oxide-to-SiC interface or by the presence of donor-like states located close to the conduction band of SiC.

For the explanation of the difference between the ideal current-voltage characteristics and the experiments (Fig.1), we first used the conventional NIT model in our simulations and adapted its parameters accordingly. As shown in Fig.2, excellent agreement between simulated and experimental results was achieved with the parameters summarized in Table 1. Most of the values are in agreement with the values reported in literature [1,4]. However, to be able to explain the low threshold voltage in the measurements, we need a value for the fixed charge density which is more than twice the value usually assumed in literature.

### New suggested NIT model

To avoid the high fixed charge density, we suggest an extension of the conventional NIT model. We propose the solution similar to the semiconductor with donor impurities, and in addition to the acceptor-like traps, we introduce also donor-like electronic states in the upper half of the SiC bandgap which provide positive charge at the gate-oxide-to-SiC interface in the sub-threshold mode of operation. For the sake of simplicity, we assume donor-like traps with a single energetic level close to the conduction band of SiC. After adding them in the simulation, we got an NIT model for the SiC/SiO₂ interface which also shows excellent agreement with the experiments. The parameters used for the simulation shown in Fig. 3 are summarized in Table 2. The newly introduced donor states lead to a decrease of the fixed charge density and of the density of near-interface acceptor traps in the vicinity of the SiC conduction band edge in comparison with the conventional NIT model.

The energetic properties of some donor type impurities in SiC were investigated in literature [5-7] by nitrogen (N) or sulfur (S) implantation into SiC/SiO₂ MOS capacitors. The N-implanted 3C-SiC MOS capacitors indicated the existence of two different types of interface traps, located at different energetic positions. It was proposed that N atoms are incorporated only in part of the

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### Table 1. Model parameters used in the conventional NIT model

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Units</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive fixed charge ($N_i$)</td>
<td>cm⁻²</td>
<td>3.42×10¹²</td>
</tr>
<tr>
<td>Midgap trap density of acceptor states ($D_{it_{mid}}$)</td>
<td>cm⁻²·eV⁻¹</td>
<td>2.4×10¹¹</td>
</tr>
<tr>
<td>Band-edge trap density of acceptor states ($D_{it_{edge}}$)</td>
<td>cm⁻²·eV⁻¹</td>
<td>4.6×10¹³</td>
</tr>
<tr>
<td>Acceptor peak trap energy ($E_c-E_{peak}$)</td>
<td>eV</td>
<td>0.02</td>
</tr>
<tr>
<td>Acceptor band-tail energy ($\sigma$)</td>
<td>eV</td>
<td>0.067</td>
</tr>
</tbody>
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Fig.2. Measurements (symbols) compared to simulations (lines) with the conventional NIT and mobility degradation models.
carbon-clusters at the 3C-SiC/SiO$_2$ interface and act as positively charged interface donors, slightly reducing the NIT density. In analogy, we assume that nitrogen introduced by the N$_2$O oxidation and N$_2$ annealing may passivate interface states [8,9]. But we also propose that a small amount of N atoms, located near the SiC/SiO$_2$ interface, gives donor type impurity levels close to the SiC conduction band. In accordance with the typical behavior of donor impurities, they will provide additional electrons to the conduction band of SiC, leading to a decrease of the threshold voltage. However, to explain the donor traps, we cannot exclude a contribution from individual carbon complexes at the interface.

Table 2. Model parameters used in the new suggested NIT model

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Units</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive fixed charge ($N_f$)</td>
<td>cm$^{-2}$</td>
<td>$1.3 \times 10^{12}$</td>
</tr>
<tr>
<td>Midgap trap density of acceptor states ($D_{it,mid}$)</td>
<td>cm$^{-2}$·eV$^{-1}$</td>
<td>$2.4 \times 10^{11}$</td>
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<tr>
<td>Band-edge trap density of acceptor states ($D_{it,edge}$)</td>
<td>cm$^{-2}$·eV$^{-1}$</td>
<td>$3 \times 10^{13}$</td>
</tr>
<tr>
<td>Acceptor peak trap energy ($E_{c-E_{peak}}$)</td>
<td>eV</td>
<td>0.02</td>
</tr>
<tr>
<td>Acceptor band-tail energy ($\sigma$)</td>
<td>eV</td>
<td>0.067</td>
</tr>
<tr>
<td>Density of donor traps</td>
<td>cm$^{-2}$</td>
<td>$2 \times 10^{12}$</td>
</tr>
<tr>
<td>Donor trap energy ($E_{c-E_{peak}}$)</td>
<td>eV</td>
<td>0.045</td>
</tr>
</tbody>
</table>

Summary

A TCAD simulation analysis has been performed to understand the physical mechanisms determining the electrical performance of $n$-channel 4H-SiC MOSFETs. Two models of the Near-Interface Traps were presented and compared with experimental results. Besides the conventional model with acceptor-like traps, a new model was considered which assumes two types of traps: donor-like and acceptor-like traps, both energetically located near the conduction band of 4H-SiC substrate. Both of the models show a good agreement with experiments assuming different concentrations of the fixed charge and defect trap densities. Based on concepts presented in literature, we relate donor traps to donor impurities located at or near the SiC/SiO$_2$ interface or to some over-stoichiometric carbon atoms. Further investigations are needed to quantify the concentration of fixed charges and of donor type defects after particular processing of SiC-MOSFETs.

Acknowledgments

This work has been carried out in the framework of the project MobiSiC (Mobility engineering for SiC devices) and supported by the Program Inter Carnot Fraunhofer (PICF 2010) by BMBF (Grant 01SF0804) and ANR.

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