Correlation of Interface Characteristics to Electron Mobility in Channel-implanted 4H-SiC MOSFETs

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Abstract. To study mobility limiting mechanisms in (0001) 4H-SiC, lateral n-channel MOSFETs in p-implanted wells on n-type epitaxial layers were manufactured and additionally selectively shallow implanted with different nitrogen (N) doses in the channel region. The mobility was found to be limited by Coulombic scattering at low electric fields. Further surface roughness scattering was considered as a possible mobility degradation mechanism at high electric fields. First investigations of the SiC surface by atomic force microscopy (AFM) in the channel region after implantation, annealing, and gate oxide removal revealed a rather rough topology. This could lead to fluctuations in the surface potential at the SiC/SiO₂ interface, thus accounting in part for surface roughness scattering.

Introduction

Silicon carbide is the only compound semiconductor having the ability to grow a native oxide and due to its wide band gap it is well suited for high temperature applications. As the breakdown field of SiC is one order of magnitude larger compared to that of silicon, it is also an attractive material for high power applications [1]. Moreover high frequency applications would benefit from the twice as high saturation velocity of electrons compared to Silicon. The SiC/SiO₂ interface, however, suffers from a high density of interface states in comparison with Si MOS which is detrimental for the inversion layer mobility in MOSFETs with surface channels. In this paper we investigate the effect of nitrogen (N) implantation into the MOSFET channel region prior to thermal oxidation on the field-effect mobility ($\mu_{FE}$) of inversion charge carriers. By further considering the temperature dependent behavior of $\mu_{FE}$ as well as the sheet carrier density in the channel region and the physical atomic roughness of the SiC/SiO₂ interface, the dominant mobility limiting mechanisms at low and high electric fields were examined.

Device Structure and Fabrication Process

Fig. 1 shows a schematic cross-section of the manufactured lateral n-channel 4H-SiC MOSFET. The MOSFETs were fabricated on p-implanted Si-face n-type epitaxial layers (net donor concentration $8 \cdot 10^{15}$ cm⁻³) on n⁺ substrates (4° off-axis) from Cree, Inc. After the deposition of a 50 nm thick scattering oxide the source and drain regions were selectively box implanted with N. Subsequently, multiple aluminum (Al) implantations were carried out to obtain suitable, box shaped, p-type wells (Al concentration of $5 \cdot 10^{17}$ cm⁻³) for the fabrication of n-channel MOSFETs. Three samples (N1-N3)
were then shallow implanted in the channel regions of the MOSFETs with different doses of N ions (e.g. N1: 5·10^{12} \text{ cm}^{-2}; N2: 1·10^{13} \text{ cm}^{-2}; N3: 5·10^{13} \text{ cm}^{-2}) at an energy of 20 keV. Sample N0 was not implanted in the channel region. Following the implantations and the removal of the scattering oxide, the wafers were annealed in Ar ambient at a temperature of 1973 K for 30 min. For the annealing step, a capping layer was employed to reduce surface degradation. A 500 nm thick field oxide was deposited by CVD and patterned to open the gate and contact regions of the devices. Thereafter the gate oxide was grown by dry oxidation in N_{2}O atmosphere at 1553 K for 150 min and subsequently annealed at the same temperature for 30 min under N_{2} ambient. The resulting interface between the 26.5 nm thick SiO_{2} and the SiC epitaxial layer was located at the maximum N concentration of the Gaussian like channel implantation profile. Phosphorus-doped polycrystalline silicon was deposited by LPCVD and patterned to form the gate electrodes. For the fabrication of the source, drain, bulk, and p-well contacts, SiC was alloyed with nickel by rapid thermal annealing at 1373 K for 2 min and subsequently a metallization stack containing titan and platinum was deposited and patterned. The channel length and width of the investigated MOSFETs were 10 µm and 100 µm, respectively.

Results and Discussion

The electrical characterization of MOSFET devices fabricated with and without N implantation before gate oxidation is presented in this paragraph. Fig. 2 shows the measured drain current ($I_D$) as a function of the gate voltage ($V_G$) for samples N0, N1, N2, and N3. For three samples the temperature ($T$) dependence of the transfer characteristics is also shown. The measurements were performed with a constant drain voltage ($V_D$) of 100 mV in the temperature range of 303 -553 K. The field-effect mobilities ($\mu_{FE}$) of all samples were calculated from the collected $I_D$-$V_G$ characteristics and are shown in Fig. 3 for several temperatures as a function of $V_G$. For all samples the drain current as well as the peak field-effect mobility of the 4H-SiC MOSFETs increases with N implantation dose or temperature. Furthermore, a characteristic behavior of $\mu_{FE}$ is observed for all samples and temperatures: With increasing $V_G$ the low-field mobility raises, reaches its peak value, and subsequently decreases in the high-field regime to a distinct value that is virtually equal irrespective of N doping or temperature. This behavior is more pronounced at elevated temperatures or higher N concentrations in the MOSFET channel region. From the $I_D$-$V_G$ characteristics the threshold voltage ($V_{TH}$) was estimated by linear extrapolation of the linear region down to the voltage axis. In Fig. 4 the peak $\mu_{FE}$ values are correlated with the extracted $V_{TH}$ values. In contrast to the increase of $\mu_{FE}$, $V_{TH}$ is significantly reduced by a raising N implantation dose or temperature. From Hall effect measurements on MOS gated Hall bar structures that were fabricated together with the presented MOSFETs the sheet carrier density in the channel region was extracted (Fig. 5). The structure of the devices and the measurement setup are described elsewhere [2]. As expected, the carrier density increases with

![Fig. 2: Comparison of transfer characteristics measured at different temperatures on samples with and w/o N implantation in channel region.](image1)

![Fig. 3: Field-effect mobility as a function of $V_G$ calculated for all samples employing the $I_D$-$V_G$ characteristics shown in Fig. 2.](image2)
increasing gate voltage. However, the slopes ($\partial n_{\text{inv}} / \partial V_G$) amount to about $4 \cdot 10^{11} \, \text{V}^{-1} \text{cm}^{-2}$. This value being by a factor of about two smaller than the ideally expected slopes ($C_{\text{ox}}/q=8.1\cdot10^{11} \, \text{V}^{-1} \text{cm}^{-2}$) indicates that approximately half of the available charge is trapped in interface states. This reduces on the one hand the amount of charges available for conduction and on the other hand gives rise to a large amount of Coulomb scattering centers at the interface.

Based on the above observations, we conclude that the increase in low-field mobility is mainly due to a decreased amount of Coulombic scattering of free charges. This decrease is caused by two different effects. First, a reduction in the bulk potential ($\Phi_B$) achieved by either N implantation (e.g., counter doping of the channel region) or by an increase in measurement temperature, induces a smaller amount of electrons trapped in interface states at a given sheet carrier density. Thus a decreased amount of Coulomb scattering centers is present at the point of inversion (e.g., band bending $\psi_S = 2\Phi_B$). This is also consistent with the observed decrease of $V_{\text{TH}}$, because for the achievement of the inversion condition only a smaller amount of net negative charge at the interface must be counterbalanced by an equal amount of positive charges at the gate [3]. Second, the counter doping with N and, to a smaller extent, also the increase in temperature reduce the spatial confinement of the current density at the SiC/SiO$_2$ interface [1] whereby an increase in the current density farther from the interface is facilitated. The second effect reduces the Coulomb scattering because this mechanism becomes less effective very quickly with increasing distance from the SiC surface [4]. Both effects can interfere with each other in our samples, whereby the first is dominant in sample N0 and the second is essential for the increase of $\mu_{\text{FE}}$ in the N doped samples.

Contrary to the low-field mobility, the high-field mobility appears to not be dominated by Coulombic scattering as we observe only one distinct field-effect mobility ($\mu_{\text{FE}}\approx12.9\pm0.9 \, \text{cm}^2\text{V}^{-1}\text{s}^{-1}$) value at the maximum gate voltage of 16 V irrespective of temperature or the net doping concentration in the channel region (Fig. 6). Further the sheet carrier density at high fields is much larger compared to the low field case (Fig. 5). Similarly to Si/SiO$_2$ systems where an increased density of free electrons enhances the well-studied effect of screened Coulomb scattering in surface channels [5], it is assumed that the amount of Coulomb scattering in the SiC/SiO$_2$ case is likewise reduced. Hence Coulomb scattering cannot be the dominating scattering mechanism. Instead it must be one that is not dependent from temperature. In this respect surface roughness scattering comes into consideration as it is anticipated that this mechanism does not depend from temperature [6].

Figure 4: Comparison of peak field-effect mobility as a function of threshold voltage for all analyzed samples and temperatures.

Figure 5: Sheet carrier density measured at room temperature as a function of $V_G$ for samples N0, N1, N2, and N3.

Figure 6: Field-effect mobility at $V_G=16 \, \text{V}$ in correlation to the respective peak field-effect mobility for all samples and temperatures.
believed that “surface roughness” could be explained by a physical atomic roughness at the SiC/SiO₂ interface [4]. Also the thermal oxidation in an nitric oxide (NO) containing atmosphere might lead to a more rough surface compared to the thermal oxidation in dry O₂ [7]. In a first attempt to quantify the physical roughness of the SiC/SiO₂ interface in our devices, the gate oxide in the channel region of the devices (N₀ and N₃) was removed by wet etching in highly diluted hydrofluoric acid (HF) (concentration ≤ 1.5%) and the bare SiC surface was immediately characterized by AFM, whereby an AFM tip with a tip radius of curvature below 5 nm was employed to enhance the lateral resolution. This procedural method revealed a rather rough surface topology with absolute step heights (Δₐₘₖₖ) of up to 1.2 nm. These nanosteps were irregularly distributed, whereby the absolute distance (Lₐₘₖₖ) between them was in the range of 5-95 nm. Yet further complementary measurements are needed for consolidation and quantification of errors made by the AFM surface characterization method or induced by the employed wet etching technique. Our preliminary AFM results, however, allow at least for the assumption that the physical atomic roughness of the SiC/SiO₂ interface cannot be excluded as one determining component that induces irregular variations in the surface potential at the 4H-SiC/SiO₂ interface, thus accounting in part for the small high-field mobility in our samples. The contribution of a second scattering mechanism know to have a significant dependence on the surface electric field, namely acoustic phonon scattering, could also be crucial for the reduced high-field mobility. However, its influence couldn’t be quantified in this study as further mobility measurements at higher temperatures (> 550 K) have to be carried out.

Summary

We have investigated the field-effect mobility and the sheet carrier density in n-channels of 4H-SiC MOSFETs as a function of temperature and N implantation dose in the channel region. We found for all investigated devices that Columbic scattering at trapped charges at the SiC/SiO₂ interface is the determining factor for low-field mobility and surface roughness scattering for high-field mobility. The atomic roughness of the SiC/SiO₂ interface determined by AFM was discussed to be one possible origin of the observed surface roughness scattering.

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References

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