3D stacked vertical nanowire transistors for novel energy-efficient logic architecture.

Laboratory : LAAS-CNRS, Toulouse, FRANCE.

Data size and functionality requirements for computing continue to increase, and this is particularly true for emerging distributed computing paradigms for the Internet of Things, such as Edge Computing and Fog Computing. Vertical gate-all-around nanowire field effect transistors (Nanoscale, 2013, 5, p. 2437) currently under development allow a truly 3D layout configuration to continue to scale gate length and benefit from scaling improvements to energy-efficiency. This architecture is a natural extension of current FinFET architectures, where the gate, defined vertically, is totally wrapped around the conduction channel of the transistors, leading to a strong reinforcement of the electrostatic control of the carriers moving through the channel. Vertical integration is a particularly attractive approach because of its intrinsic 3D nature, which is more favorable to scale the contacted gate pitch i.e. scaling of the gate length and contact area.

In the framework of a French research project (ANR LEGO) and with research partners IMS (Bordeaux) and INL (Lyon), the Material and Processes for Nanoelectronic (MPN) group at LAAS aims to research novel non-conventional transistor architecture based on stacked vertical NWFETs to explore high-performance and energy-efficient computing paradigms. In this context we are currently looking for a (m/f) PhD student for a 3 year contract.

The goal of the thesis is to develop these stacked transistor architectures based on vertical nanowire arrays in close collaboration with design (INL) and modelling (IMS) partners. This thesis, technology-oriented, covers a broad research spectrum from the material to the device level at the forefront of research worldwide and allows the development of a wide knowledge (materials science at the nanoscale, nanofabrication, physical and electrical characterization). This thesis will take place in the LAAS-CNRS laboratory in Toulouse (France), which has a state-of-the-art clean room facility (1500m ²) dedicated to the fabrication of micro / nano devices.

Talented, enthusiastic candidates with excellent analytical and communication skills are encouraged to apply. The candidate, MASTER graduated, will have good theoretical knowledge in materials science and / or semiconductor physics and a strong taste for experimental work.

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