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Importance of point defect reactions for the atomic-scale roughness of III–V nanowire sidewalls

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Abstract

The surface morphology of III–V semiconductor nanowires (NWs) protected by an arsenic cap and subsequently evaporated in ultrahigh vacuum is investigated with scanning tunneling microscopy and scanning transmission electron microscopy. We show that the changes of the surface morphology as a function of the NW composition and the nature of the seed particles are intimately related to the formation and reaction of surface point defects. Langmuir evaporation close to the congruent evaporation temperature causes the formation of vacancies which nucleate and form vacancy islands on {110} sidewalls of self-catalyzed InAs NWs. However, for annealing temperatures much smaller than the congruent temperature, a new phenomenon occurs: group III vacancies form and are filled by excess As atoms, leading to surface As_{Ga} antisites. The resulting Ga adatoms nucleate with excess As atoms at the NW edges, producing monoatomic-step islands on the {110} sidewalls of GaAs NWs. Finally, when gold atoms diffuse from the seed particle onto the {110} sidewalls during evaporation of the protective As cap, Langmuir evaporation does not take place, leaving the sidewalls of InAsSb NWs atomically flat.

Keywords: III–V semiconductor nanowires, {110} sidewall, surface morphology, roughness, point defect, scanning tunneling microscopy

(Some figures may appear in colour only in the online journal)

1. Introduction

Compound semiconductor nanowires (NWs) have attracted wide interest for optoelectronic and photovoltaic applications, due to their unique ability to relax strain and hence enabling the realization of a much wider range of non-lattice matched heterostructures and polytypes than in planar growth. Numerous examples of heterogeneous integrations have been demonstrated, either axially with III–V NWs directly grown

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on Si substrates [1, 2] or radially with semiconductor–semiconductor, semiconductor–ferroelectric and semiconductor metal core–shell NWs [3–6]. However, the quality of the interface, in particular in the radial configuration, where the surface to volume ratio is high, critically affects the NW properties. Hence, controlling the surface morphology and chemistry of NWs is becoming of utmost importance for tuning manifold NW properties, not only for the growth of core–shell structures, but also to prepare NWs with strong confinement effects [7] or enhanced luminescence [8].

Indeed, apparently small surface effects can have a strong impact on the physical properties of semiconductor heterostructures. For example, a pronounced roughness of the sidewall facets will reduce the sharpness of radial interfaces and increase the scattering of electrons and phonons, influencing their propagation. Also, surface steps induce a Fermi-level pinning at the NW sidewall facets, which modifies the band offsets between different axially arranged polytypes or heteromaterials [9, 10], hence influencing greatly the axial electrical conductivity and optical emission of NWs. Moreover, this pinning governs the incorporation of defects and isoelectronic impurities during lateral overgrowth, affecting the electronic properties of core–shell heterostructures.

These effects are likely to occur when the growth processes require the evaporation of chemical elements that take place in separate growth systems, implying stringent conditions to preserve the interfacial layer from contamination accumulated during the sample transfer [11]. For III–V semiconductor NWs, a smart protection scheme relies on the use of a thin arsenic amorphous layer to cap the NW sidewalls [12, 13], that can then be easily sublimated once the sample has been transferred in a different growth system. However, it is still not clear how the protective cap affects the morphology of the NW sidewalls. This is even more important in the light of very different surface morphologies observed by scanning tunneling microscopy, ranging from very rough to atomically smooth facets [14], but without good understanding thus far.

In this work, we examine clean and well-ordered (110) sidewalls of III–V semiconductor NWs with scanning tunneling microscopy (STM) and spectroscopy (STS) after the sublimation of an As protective cap. We find pronounced differences in the morphology and roughness of NW sidewalls of different III–V compounds. The morphologies are shown to correlate with point defect formation and reaction processes during the sublimation of the As protective cap. These point defect-based processes lead to sidewall morphologies characterized by nucleated islands, vacancy clusters, atomically smooth sidewalls, as well as to highly off-stoichiometric or perfectly stoichiometric surfaces depending on annealing and Fermi-level position at the NW surface.

2. Methods

For the experiments, InAs, GaAs and $InAs_{1-x}Sb_x$ NWs were synthesized by molecular beam epitaxy with seed particles to drive the NW growth in the vapor–liquid–solid regime. In and Ga droplets were used for the growth of self-catalyzed InAs and GaAs NWs on [111]-oriented Si substrates covered with a native oxide layer at the surface. As described in [15], optimized conditions with oxide thickness of 0.9 nm were chosen to obtain the highest yield of vertical growth. The growth of InAs NWs was done at 0.02 monolayer per second, given as equivalent to the growth rate on planar GaAs, with an As_4 partial pressure of 3.6×10^{-7} mbar, an In partial pressure of 4.1×10^{-8} mbar and a temperature of 420 °C. The growth of GaAs NWs was carried out at a nominal growth rate of 0.3 Å s^{-1}, with an As_4 partial pressure of 2.5×10^{-6} mbar, a Ga partial pressure of 1.4×10^{-7} mbar and a temperature of 620 °C. At the end of the growth, the In and Ga droplets were consumed by closing the In or Ga shutter for 30 min under As_4 flux. Then, the As_4 flux was stopped, what reduced the As-related pressure substantially, and the temperature was lowered to room temperature. At room temperature, the As_4 flux was opened again and the NWs were capped with a 10–20 nm thick amorphous As layer for protection against air exposure (oxidation). A high yield of vertical NWs grown along the ⟨111⟩ direction was obtained, with a diameter distribution between 60 and 90 nm [16]. $InAs_{1-x}Sb_x$ NWs and GaAs NWs were also grown with gold seed particles, as thoroughly described in [12] and [17]. The capping procedure was similar except that the gold seed particle was left at the end of the growth and embedded in the As capping layer.

After the growth, the NWs were investigated with a Jeol 2200 FS scanning transmission electron microscope (STEM) operating at 200 keV and with a low-temperature scanning tunneling microscope working at 77 K in ultrahigh vacuum (UHV). The STEM analysis required to work with cleaved and dispersed NWs in toluene that were dropcasted onto E-chip supports (Protochips). The annealing of the NWs to sublimate the As-capping layer was performed *in situ* and the temperature of the E-chip in the STEM was measured with a thermocouple. For the STM characterization, the sublimation process was performed in the preparation chamber connected to a low-temperature scanning tunneling microscope with a base pressure lower than 10^{-10} mbar. The substrate that was used to grow the NWs was annealed by direct current heating. The As desorption was monitored by mass spectrometry and the temperature of the sample was probed with a pyrometer, yielding an uncertainty of ±10 °C on the substrate temperature. While the pressure increased around $2–5 \times 10^{-10}$ mbar for a few tens of seconds and then decreased, we usually kept the sample heating for 30 min. At the end of this process, the NWs were transferred to a *n*-type Si(111) substrate coated with a thin layer of Ag. The transfer was performed by mechanical cleavage of the NWs without interruption of UHV [18], to have one of the sidewalls parallel to the host substrate and accessible to the tungsten STM tip. For the STM study, we did not consider the base or the top region of the NWs, since the morphology of these regions can be different from the rest of the NWs. Tunneling spectroscopic curves were acquired with an open feedback loop at constant tip-sample separation.

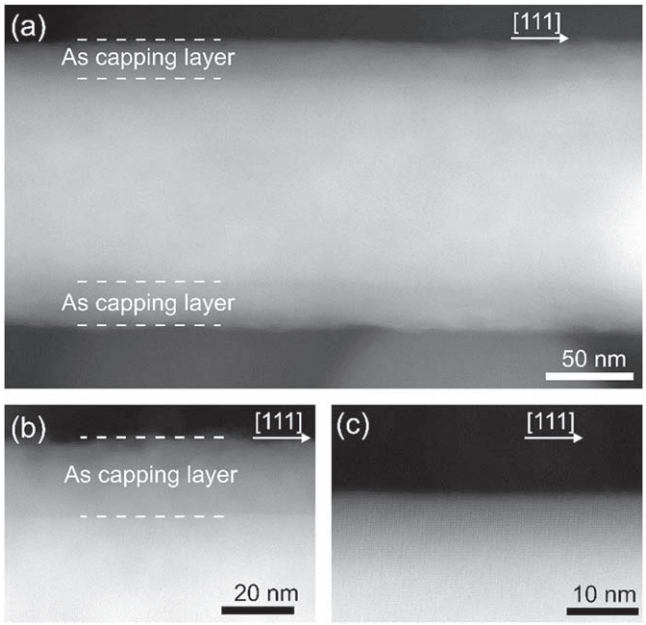

Figure 1. (a) STEM image of a self-catalyzed GaAs NW capped with a thin protective layer of amorphous As. (b) and (c) TEM images of the same GaAs NW after the annealing of the sample at 250 °C for 10 min and then 270 °C for 10 min. At 250 °C, the amorphous As cap is still present and blurs the NW's atomic structure (b). In contrast, at 270 °C the As cap evaporated fully (c), revealing the underlying atomic structure of the NW.

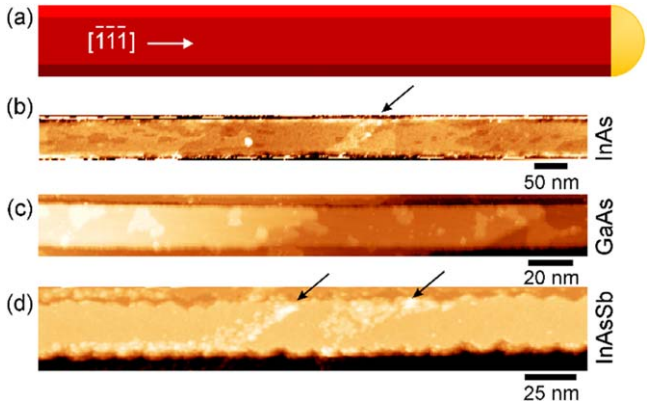

Figure 2. STM images of the {110} sidewall of (a) an In-catalyzed InAs NW, (b) a Ga-catalyzed GaAs NW and (c) a Au-catalyzed $InAs_{0.9}Sb_{0.1}$ NW obtained after the sublimation of the As capping layer at 370 °C–380 °C, tunneling conditions: (a) $V_{sample} = +3.0$ V/$I_{tunneling} = 10$ pA, (b) $V_{sample} = -4.0$ V/$I_{tunneling} = 20$ pA, (c) $V_{sample} = -3.0$ V/$I_{tunneling} = 10$ pA. The arrows point to defective areas.

3. Results

In order to determine the range of temperatures that enable the complete sublimation of the As protective cap, temperature-dependent STEM experiments were first performed with self-catalyzed GaAs NWs. Figure 1(a) shows a typical STEM image of such a GaAs NW capped by an amorphous As capping layer. The capping layer is identified from its slightly darker contrast in the upper and lower parts of the NW in comparison with the GaAs core. The thickness of the capping layer is 20 nm. Heating the NW at 250 °C for 10 min does not produce any significant modification of the protective cap (figure 1(b)). Further annealing at 270 °C for 10 min leads to the disappearance of the dark As shell and the appearance of the NW atomic lattice in the STEM image, as shown in figure 1(c). Both observations indicate the sublimation of the protecting As cap. However, annealing at this temperature was found to leave a lot of defective areas in the STM images of the NWs sidewalls. Therefore, for the subsequent STM analyses, the As capping layer was always sublimated above 310 °C–320 °C and below 370 °C–380 °C. The upper limit corresponds to the congruent evaporation temperature of InAs [19].

Figure 2 shows an overview of STM images for three different III–V NWs after the sublimation of the As-capping layer at the maximum temperature of 370 °C–380 °C allowed for this study. The morphologies of the sidewalls for the NWs appear different, despite the same ⟨110⟩ orientation of the sidewalls and similar conditions to sublimate the capping layer. First, the InAs and GaAs NWs have straight sidewalls while the $InAs_{1-x}Sb_x$ NW appear with sawtooth-like sidewalls. This difference has been explained by the epitaxial overgrowth of the sidewalls [20]. ⟨111⟩-oriented NWs have initially twelve alternating {110} and {112} sidewalls. However, if overgrowth takes place, the grooves induced by the {111}-A and B-type facets in the {112} planes, which give rise to the sawtooth-like shape, are filled in and the {112} planes becomes narrower. As a result, the {110} sidewalls almost connect with each other giving rise to straight edges along the growth axis.

More importantly for this study, we compare the roughness of the {110} sidewalls. The InAs NW sidewall consists of propagating terraces along the growth direction, with pits sparsely distributed into the terraces (figure 2(b)). We note the presence of a small defective area, which is presumably a damaged region that might affect the complete removal of the As capping layer in its vicinity. The GaAs NW sidewalls exhibit terraces also. But opposite to the pits observed on the InAs NW sidewalls, islands appear on top of theses terraces (figure 2(c)). Interestingly, the majority of the islands are connected to the sidewall and terrace edges, whereas the pits seem to be randomly distributed on a terrace. In contrast to the InAs and GaAs NWs, the $InAs_{1-x}Sb_x$ NW sidewall is atomically flat, except in two small defective areas (figure 2(d)). While the absence of terraces might be related to the limited duration of the lateral overgrowth process as compared with the InAs and GaAs NWs, this third example shows that the {110} sidewalls can also exist without any pits or islands.

In order to get further insight into the origin of the formation of these clusters and islands, figure 3 highlights the height profiles measured on the sidewalls of the self-catalyzed InAs and GaAs NWs. At the surface of the InAs NW, the pits have a depth of about 2 Å, whereas the islands that are found on the GaAs NWs show a height of 2 Å. These heights correspond to the separation of single atomic (110) planes in

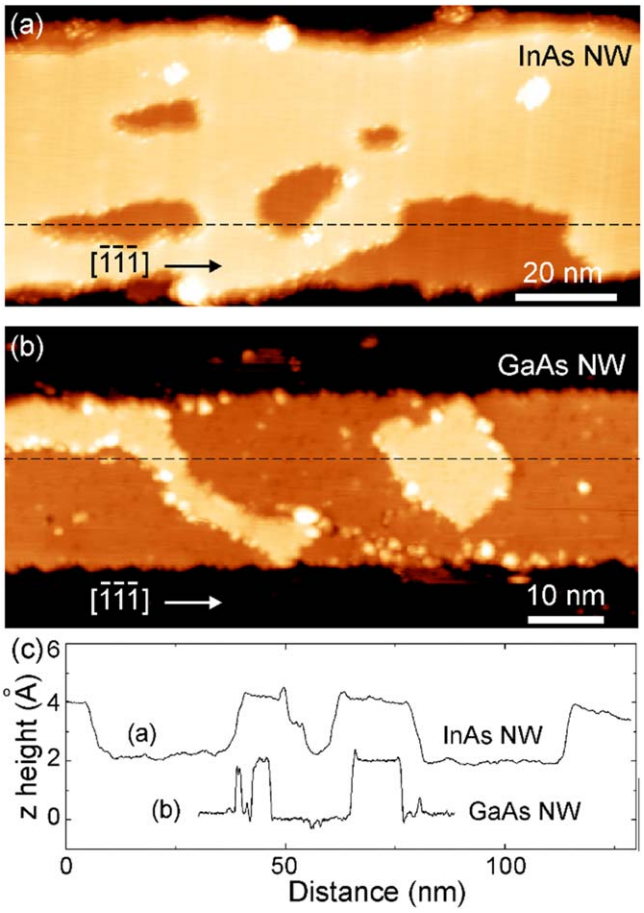

Figure 3. STM images of the {110} sidewall of self-catalyzed (a) InAs and (b) GaAs NWs after the removal of the As capping layer at 370 °C–380 °C. (c) Height profiles measured along the horizontal lines in (a) and (b). Tunneling conditions: $V_{\text{sample}} = +2.0$ V (a)/-3.5 V (b), $I_{\text{tunneling}} = 20$ pA. Vacancy islands are found to form on InAs NW sidewalls, whereas islands nucleate on GaAs NW sidewall at edges.

InAs and GaAs crystals, meaning that single-layer vacancy clusters or islands with monoatomic step height were formed.

In order to get further insight into the origin of the formation of these clusters and islands, we examined surfaces of III–V semiconductor bulk crystals. Figures 4(a)–(c) shows atomically flat (110) surfaces of a cleaved *p*-type InP crystal, a cleaved *p*-type GaAs crystal and a cleaved *n*-type GaAs crystal respectively. All three crystals show single vacancies, but depending on the doping of the crystals, the nature of the vacancies is different. Group V vacancies are observed in the filled state images of figures 4(a) and (b), while Ga (group III) vacancies are visible in the unoccupied state image of figure 4(c), consistent with previous studies [21–23]. We note that the STM image of the *p*-type InP surface was acquired after sample annealing at 205 °C for 42 h in UHV. Upon further annealing at 300 °C for 6 h, the *p*-type InP surface shows the formation of pits (figure 4(d)), similar to those produced upon exposure to electrons, photons or ions [24–26].

For surfaces initially covered with a thin As capping layer and then annealed to desorb the capping layer, such as the InAs (001) surface in figure 4(e) and the GaAs (110) surface in figure 4(f), the same pits are also found. Once the amorphous capping layer has been desorbed, desorption of atoms from the crystal occurs and gives rise to the holey surface seen on the InAs NW sidewalls. The surface morphology is fully consistent with the formation of vacancy clusters resulting from stoichiometric Langmuir evaporation of group III and group V elements. Both elements leave the surface at equal fluxes because the annealing temperature is lower than the congruent temperature [27].

In contrast, the GaAs NW sidewalls do not show a pit-dominated morphology, but rather an island morphology. Understanding this requires a deeper examination of the possible presence of defects on the GaAs NW sidewalls. The atomically resolved STM image of figure 5(a) corresponds to a filled state image and shows rows of As atoms on the {110} sidewall of the NW. Interestingly, atomically confined protrusions at Ga lattice sites are seen between the As rows. Counting their number yields a surface density of protrusions of 4×10^{13} cm^{-2}. These defects do not cause a change of contrast in their surroundings and can be found next to each other in the same row, suggesting that they are uncharged. We anticipate that the protrusions correspond to As atoms substituted to Ga atoms. This is supported by their comparison with the STM image of an As_{Ga} antisite defect in the surface layer simulated with density functional calculations of the integrated filled local density of states [28]. As we do not observe any contrast associated with subsurface As_{Ga} antisite defects as found previously in low-temperature grown GaAs planar layers as well as GaAs NWs [29–31], our result suggests that the antisites are exclusively formed at the GaAs surface during the post-growth decapping process.

An additional insight into the post-growth mechanism is provided by the statistical analysis of the one-monolayer-height islands. The Abott curve calculated with the STM image shown in the inset of figure 5(c) reveals that 18% of the sidewall is covered with islands. As the cation concentration at the GaAs (110) surface is 2.2×10^{14} cm^{-2}, it means that 4×10^{13} cm^{-2} Ga atoms are necessary to form these islands. This quantity corresponds exactly to the Ga atoms substituted by the As_{Ga} antisites.

4. Discussion

In order to explain the different morphologies obtained for the InAs NWs and the GaAs NWs despite identical post-growth treatments, we recall that the morphology is governed by the atomic processes occuring during the annealing procedure used to desorb the As cap from the NWs. These atomic processes are intimately related to point defects at the sidewall surfaces. It is well known that the types of point defects formed on III–V (110) surfaces are highly sensitive to the position of the Fermi level [32–34]. Since the formation process of point defects during desorption is a kinetically limited process, we cannot base the discussion on equilibrium energies of point defects, but rather need to consider the formation barriers. Experimentally it has been shown that

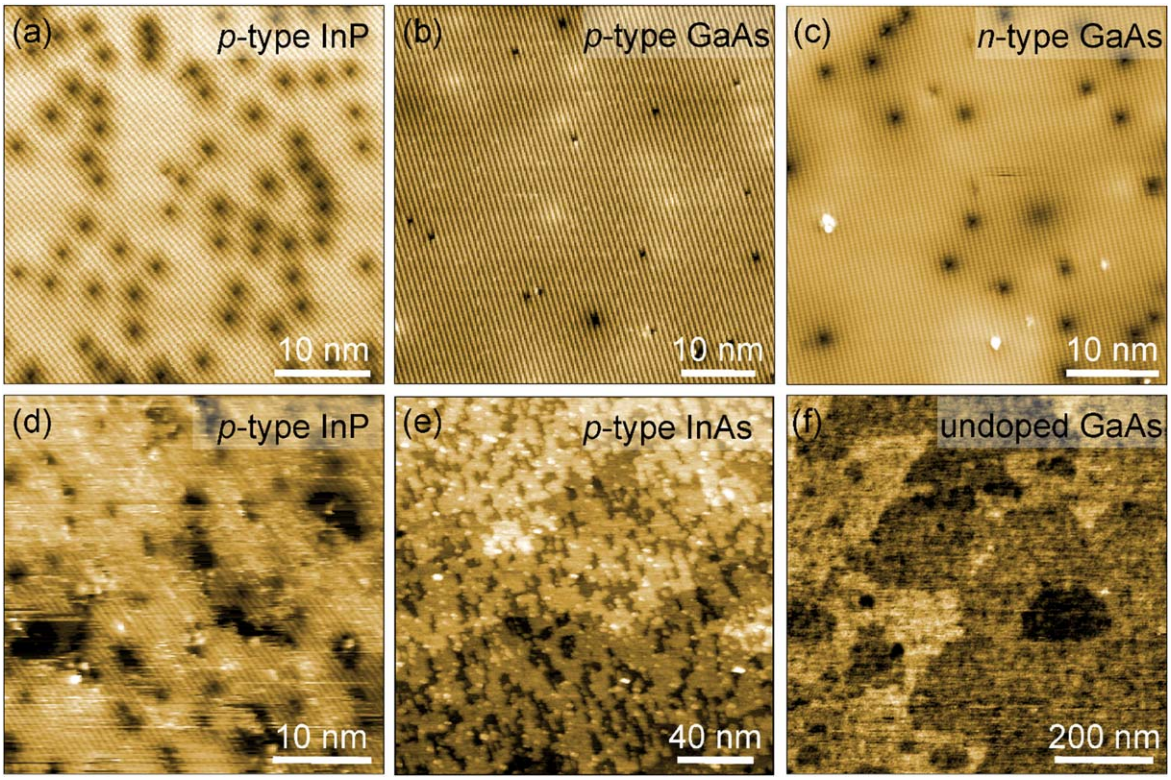

Figure 4. STM images of (a) a *p*-type InP(110) crystal annealed at 200 °C for 42 h in UHV, (b) a *p*-type GaAs (110) crystal, (c) a *n*-type GaAs (110) surface, (d) a *p*-type InP (110) surface annealed at 300 °C for 6 h in UHV, (e) a *p*-type InAs(001) crystal, initially capped with As and annealed at 400 °C for 2 h, (f) an undoped GaAs (110) crystal initially capped with As and annealed at 450 °C for 4 h in UHV. Tunneling conditions: $V_{\text{sample}} = -2.7$ V (a), −2.6 V (b), +1.2 V (c), −2.8 V (d), +1.5 V (e), +2.0 V (b); $I_{\text{tunneling}} = 800$ pA (a), 600 pA (b), 300 pA (c), 600 pA (d), 10 pA (e), 10 pA.

negatively charged group III (positively charged group V) vacancies form kinetically on *n*-type (*p*-type) surfaces even at room temperature [21–23]. No other point defect, such as antisite or adatom, is experimentally found to form thermally in significant concentrations on (110) surfaces. This is confirmed by the defects visible in figures 4(a) and (c).

Therefore, we performed tunneling spectroscopy measurements on sidewalls of the self-catalyzed InAs and GaAs NWs in order to determine the electrical nature of the sidewalls. For the GaAs NWs, the band edges are clearly resolved in figure 6: at negative (positive) sample voltages, the branches of the current correspond to a tunneling out of (into) the valence (conduction) band states. The Fermi level position, measured at 0 V, is found midgap, 0.75 eV above the valence band edge, in agreement with a previous study which attributed this position to a pinning induced by the surface steps [9]. For the InAs NWs, three regions of tunneling current are also observed. In this case, the central component turning on at 0 V and extending to negative voltages is not equal to zero. This component arises from electrons tunneling out of the partially occupied conduction band, due to a pinning slightly above the conduction band minimum. This Fermi level position within the conduction band is in agreement with measurements performed on the planar InAs(110) surface [35] and InAs NW sidewall [36]. It is caused by the formation of an electron accumulation layer near the NW sidewalls, giving a *n*-type character to the sidewall.

On this basis, one can explain the atomic processes on the (110) InAs sidewall facet: during the post-growth annealing, the amorphous As cap is progressively removed. Once crystalline (110) facets become uncovered, In vacancies form. Since the annealing temperature of 380 °C is close enough to the InAs congruent sublimation temperature of 387 °C [19], the In adatoms desorb and leave behind negatively charged In vacancies [32], with weakly bonded neighboring As atoms. These neighboring As atoms can detach and form As adatoms, which desorb by forming As_2 molecules [21]. As a result, uncharged divacancies form, which, due to the lack of repulsive Coulomb interactions, migrate and agglomerate to form pits of one monolayer depth on the whole sidewall of the InAs NW. The fact that the majority of the pits do not touch the sidewall edges indicates that their nucleation occurs randomly on the sidewall facets. Note that during these processes no charging of the surface by point defects occur. Similar effects can be expected to occur when the oxidized sidewalls of InAs NWs are cleaned with atomic hydrogen at 370 °C. Indeed the morphology observed on such prepared InAs NW sidewall facets is also dominated by holes of one monolayer depth elongated along the [111] direction [37]. It should be noted that the fraction of holes on the sidewall facet is essentially determined by the annealing time, the longer the more holes.

For the GaAs NWs an analogous effect may occur: as soon as the stoichiometric GaAs surface becomes uncovered

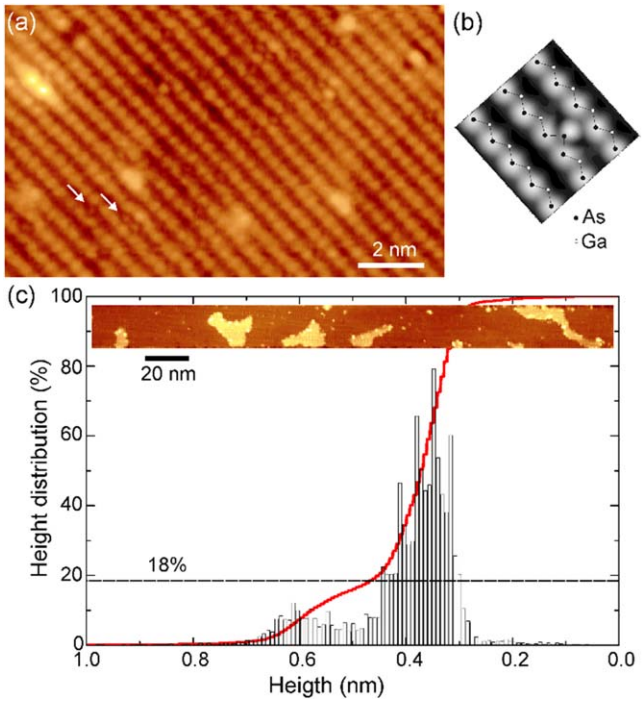

Figure 5. (a) Atomic scale STM image of the (110) sidewall of a Ga-catalyzed GaAs NW. Tunneling conditions: $V_{sample} = -3.5$ V, $I_{tunneling} = 20$ pA. The arrows point to protrusions at Ga lattice sites that correspond to a single surface As_{Ga} antisite and a pair of surface As_{Ga} antisites. (b) Calculated filled state STM image of the GaAs (110) surface including states over an energy range of 0.7 eV below the top of the valence band reproduced from [28] (c) height distribution and Abbott curve obtained for the {110} sidewall of the GaAs NW shown in the inset (tunneling conditions: $V_{sample} = -4.0$ V, $I_{tunneling} = 20$ pA). The horizontal dashed line indicates the fraction of the total area that corresponds to the bright islands seen in the STM image of the inset.

during As decapping, negatively charged Ga vacancies form for undoped and *n*-type materials [22, 38]. However, in contrast to InAs, the annealing temperature used to desorb the As capping layer is much lower than the congruent sublimation temperature of GaAs [7, 27, 39], preventing the Ga adatoms to desorb. As a result, for the following discussion, we need to take into account the presence of negatively charged Ga vacancies and Ga adatoms combined with high concentrations of As adatoms originating from the amorphous As cap. Their joint presence inevitably leads to point defect reactions: a simple formation of negatively charged Ga vacancies would lead to a negative charging of the NW sidewall facets, which would quickly undermine further vacancy formation, due to repulsive Coulomb interactions. The observation of surface antisite defects in the STM image of figure 5(a) indicates that the negative charge of a Ga vacancy can be removed by inserting an As adatom on a Ga lattice site to form an uncharged As_{Ga} antisite defect in the surface layer. This point defect reaction is very likely to happen, due to the As rich conditions created by the As cap and also energetic reasons. For midgap Fermi energies in our case, the formation energy of a V_{Ga}^{-}, a negatively charged As adatom, and an uncharged As_{Ga} antisite are 1.2, 1, 0, and −0.25 eV, respectively [38], hence freeing about 2.5 eV per

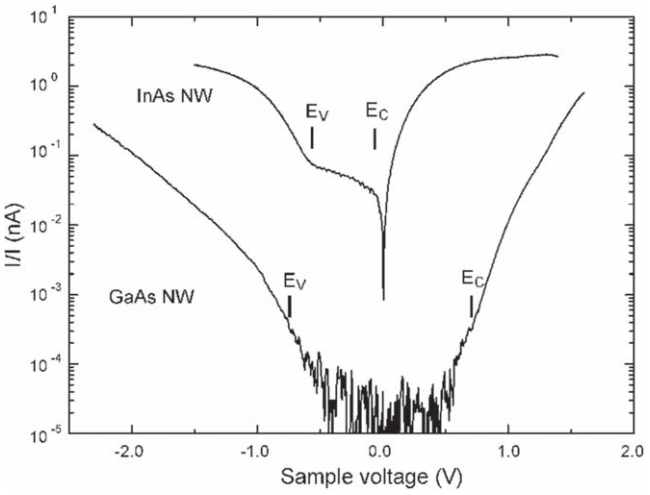

Figure 6. Tunneling spectra acquired on the {110} sidewall of self-catalyzed InAs and GaAs NWs. E_V and E_C indicate the position of the valence and conduction band edges respectively. The spectrum of the InAs NW has been shifted vertically for clarity.

formed surface antisite defect. In addition, this reaction results in charge neutrality. These antisite defects remain in the surface layer, as the barrier for inward diffusion is too high [38]. The lack of subsurface antisite defects corroborates this formation mechanism.

At this stage, we consider the Ga adatoms created during vacancy formation. Once the vacancy is filled by an As adatom, the Ga adatoms cannot jump back into the Ga vacancy nor desorb, since the temperature is too low. Hence they remain diffusing over the sidewall surface until they nucleate with As adatoms, preferentially at the NW edges, forming GaAs islands on the sidewalls. This effect is responsible for the distribution of one-monolayer-height islands observed on the sidewalls of the self-catalyzed GaAs NWs.

An intriguing aspect of this result is the degree of non-stoichiometry achievable at NW sidewall facets without formation of precipitates. In bulk GaAs, the equilibrium phase diagram only permits very small deviations from stoichiometry in the range of $\sim 10^{-3}$% at 700 °C, before precipitation occurs. The single phase area narrows even further at lower temperatures [40, 41]. Under non-equilibrium conditions in low-temperature GaAs growth, As antisite concentrations of up to 1% are reachable, but annealing leads to As precipitation [30, 42]. Here on the NW sidewall, a deviation from stoichiometry of 18% is observed at 370 °C–380 °C and no precipitate forms during annealing.

We also note that the formation of the surface antisites occurs at relatively low temperature in comparison with the congruent temperature of GaAs. This effect is not observed on the planar GaAs (110) surface which was annealed at 450 °C. Similarly, under realistic annealing temperatures, holes cannot be avoided for InAs NWs. For example, at temperatures as low as 315 °C–325 °C, As-capped self-catalyzed InAs NWs exhibit a holey surface, as shown in figure 7, meaning that the In surface atoms already desorb rather than diffuse on the sidewalls at this temperature.

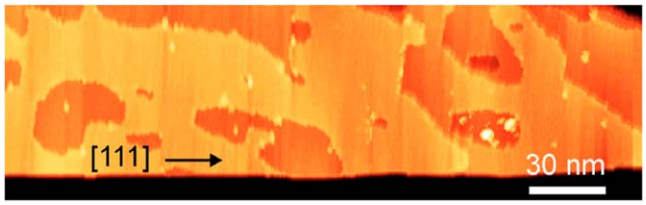

Figure 7. STM image of the {110} sidewall of a In-catalyzed InAs NWs after the removal of the As capping layer at 315 °C–325 °C. Tunneling conditions: *V* sample = +2.5 V, *I* tunneling = 10 pA.

Finally, due to the lower congruent temperature of InSb with respect to InAs [43], similar post-growth treatments should have produced a holey surface at the sidewall of the InAsSb NWs. Instead, the sidewalls are atomically flat. Although Sb behaves as a surfactant in the growth of III–V semiconductor alloys [44], we do not believe that it plays a role during the sublimation of the As layer, since it has been shown to preferentially incorporate into the surface lattice and substitute to As than diffusing at the NW surface [45]. Instead, our previous study of $InAs_{1-x}Sb_x$ NWs with STM and x-ray energy-dispersive spectroscopy analysis operated in the high-angle annular dark field STEM mode have revealed the presence of gold clusters on the NW sidewalls [12]. This result is confirmed by *in situ* temperature-dependent STEM experiments of GaAs NWs grown with Au seed particles that were protected by an As cap. Figure 8 shows a STEM image of a GaAs NW with the Au particle on top. At first, the NW and the seed particle are surrounded by the amorphous capping layer. By increasing the temperature at 250 °C, the capping layer roughens and the interface between the Au droplet and the top of the NW widens drastically, indicating the interdiffusion of As and Au atoms. In fact, the droplet becomes gradually an AsAu alloy. In concomitance, as the annealing time increases, dark features appear on the sidewall, diffusing from the Au seed particle towards the bottom of the NW. Therefore, the desorption of the As capping layer from Au-catalyzed NWs inevitably leads to the presence of gold atoms and clusters on the sidewalls. We suspect these impurities to modify the Fermi level position and to prevent the formation of vacancies, keeping the {110} sidewalls atomically flat.

5. Conclusion

We have investigated the sidewall morphology of III–V semiconductor NWs after the desorption of a protective As cap. The desorption of the As cap for self-catalyzed NWs produces two types of morphology arising from Fermi-level-dependent point defect formation and reaction. For annealing temperatures close to the congruent evaporation temperature, the formation of vacancies from the evaporation of group III and group IV elements leads to sidewalls with pits nucleating within the sidewalls. However, when the annealing temperature is much smaller than the congruent evaporation temperature, group III vacancies are formed and substituted by the excess of As atoms on the surface of the NW. The resulting

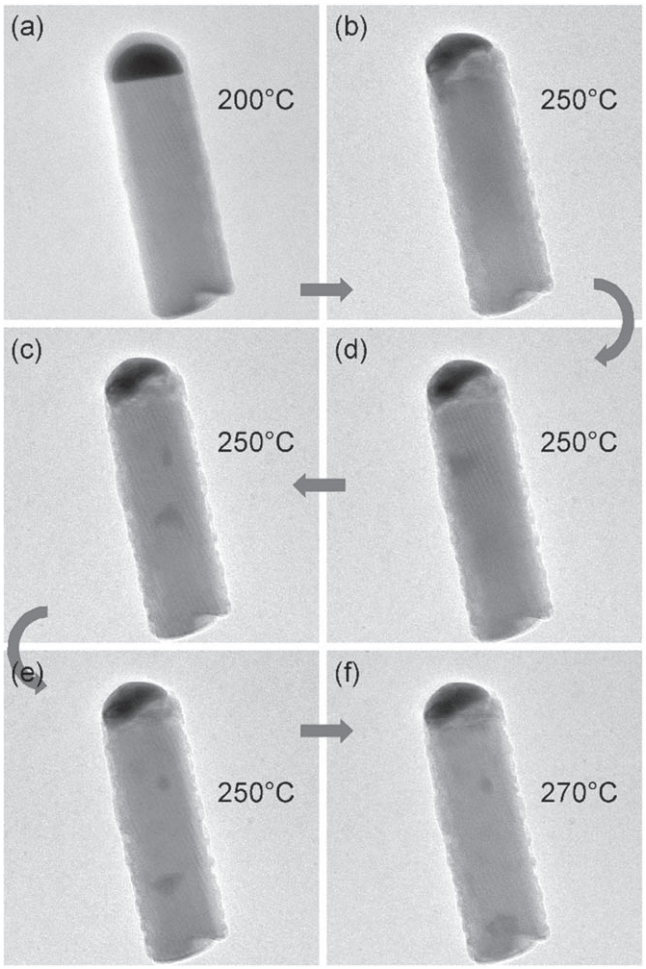

Figure 8. Sequence of temperature-dependent STEM images of an Au-catalyzed GaAs NW capped with a thin As cap. The annealing temperature is indicated in the images.

group III adatoms nucleate with excess As adatoms in islands, preferentially at the sidewall edges. We have furthermore found that a strongly enhanced solubility of excess As is achieved through these surface point defect reactions. Hence, besides the ability to relax strain much more efficiently than in planar growth, NW can also accommodate much larger deviations from stoichiometry at least at their surfaces. Finally, for gold-catalyzed NWs, Au from the seed is redistributed on the sidewalls upon desorption of the protective As cap. The Au induces a midgap pinning of the sidewalls which is anticipated to supress vacancy formation, and thereby blocks the formation of islands or vacancy pits. The results highlight the critical impact, which point defect formation and reactions have on the sidewall morphology of NWs.

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