

# Insight of surface treatments for CMOS compatibility of InAs nanowires

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## ABSTRACT

A CMOS compatible process is presented in order to grow self-catalyzed InAs nanowires on silicon by molecular beam epitaxy. The crucial step of this process is a new *in-situ* surface preparation under hydrogen (gas or plasma) during the substrate degassing combined with an *in-situ* arsenic annealing prior to growth. Morphological and structural characterizations of the InAs nanowires are presented and growth mechanisms are discussed in detail. The major influence of surface termination is exposed both experimentally and theoretically using statistics on ensemble of nanowires and density functional theory (DFT) calculations. The differences observed between Molecular Beam Epitaxy (MBE) and Metal Organic Vapor Phase Epitaxy (MOVPE) growth of InAs nanowires can be explained by these different surfaces terminations. The transition between a vapor solid (VS) and a vapor liquid solid (VLS) growth mechanism is presented. Optimized growth conditions lead to very high aspect ratio nanowires (up to 50 nm in diameter and 3 micron in length) without passing the 410 °C thermal limit, which makes the whole process CMOS compatible. Overall, our results suggest a new method for surface preparation and a possible tuning of the growth mechanism using different surface terminations.

## KEYWORDS

III-V semiconductors on silicon, InAs, nanowires, self-catalyzed growth, hydrogen preparation, growth modeling, density functional theory (DFT) modeling

## 1 Introduction

Thanks to their intrinsic properties, self-catalyzed vertical III-V nanowires (NWs) integrated on Si represent an interesting building block for the future of nanoelectronics [1, 2]. Indeed, it is possible, using wafer bonding technologies, to directly integrate Si(111) wafers on Si(001) in the Back-End-of-Line (BEOL) processes [3]. In order to achieve CMOS compatibility, nanowires have to reach some technological standards. Their growth should be vertical, self-catalyzed on Si and the CMOS BEOL standards prohibit temperature higher than 450 °C [4, 5]. If verticality and yield of self-catalyzed nanowires integrated in silicon have been widely studied [6–8], the thermal budget remains a big unaddressed issue. Indeed, if InAs or InSb nanowire growth occurs at temperatures lower than 450 °C [9–12], the substrate preparation, prior to growth, always crosses this limit. In this paper, we present a fully CMOS compatible method allowing the integration of III-V nanowires on silicon without passing the thermal BEOL limit.

Fully vertical and self-catalyzed GaAs and InAs NWs have been reported on Si(111) for both Molecular Beam Epitaxy (MBE) [6, 8, 13–20] and Metal Organic Vapor Phase Epitaxy (MOVPE) [21–26]. Whereas both materials can be grown in either systems, most convincing results for GaAs were obtained from MBE [6, 8, 13–19]; and from MOVPE in the case of InAs [22, 25–27]. For instance, Tomioka et al., using MOVPE, first demonstrated fully vertical and self-catalyzed InAs NWs on Si(111) [22], and even managed to build transistors with them [28, 29]. On the contrary, reports from MBE groups highlighted significant difficulties to match these results [9, 20, 30]. If these difficulties are supposedly due to the presence of

native oxide, and large lattice mismatches; one can also suppose that growth environment and surface preparations are crucial. Indeed, the surface reconstruction in a MOVPE chamber, due to the H<sub>2</sub> carrier gas and the high temperature *in-situ* annealing under As<sub>2</sub>, seems to be of firm importance in the process.

There are common agreements regarding the vertical and self-catalyzed growth of III-V NWs on silicon. Fontcuberta et al. [31] reported the importance of the silicon oxide thickness in the case of GaAs NWs and Tomioka et al. [22] emphasized the necessity of a complete native oxide removal for InAs NW nucleation and the creation of a Si(111)B surface before growth. In the latter case, a pre-growth high temperature annealing in the presence of H<sub>2</sub> and As<sub>2</sub> is performed in order to create a Si(111)B surface. This high temperature annealing seems to be dependent of the growth system from 950 °C for Tomioka et al. [22] down to 630 °C for Wang et al. [32]. The reported temperatures are always above 500 °C [22, 24, 25, 33]. Hence, one can conclude that the surface preparation is one of the crucial steps that need to be addressed and fully understood in order to achieve a complete CMOS compatibility.

## 2 Experimental

In this paper, we investigate the influence of the substrate preparation environment on the growth of InAs NWs by MBE and propose a fully CMOS compatible process for the integration of III-V NWs on silicon without passing the 410 °C limit. Self-catalyzed InAs NWs are grown on commercially available 2 inch NID Si(111) wafers from Siltronic in a solid-source MBE system (RIBER-MBE412). Once the native oxide is removed with the help of hydrofluoric acid (HF 5%),

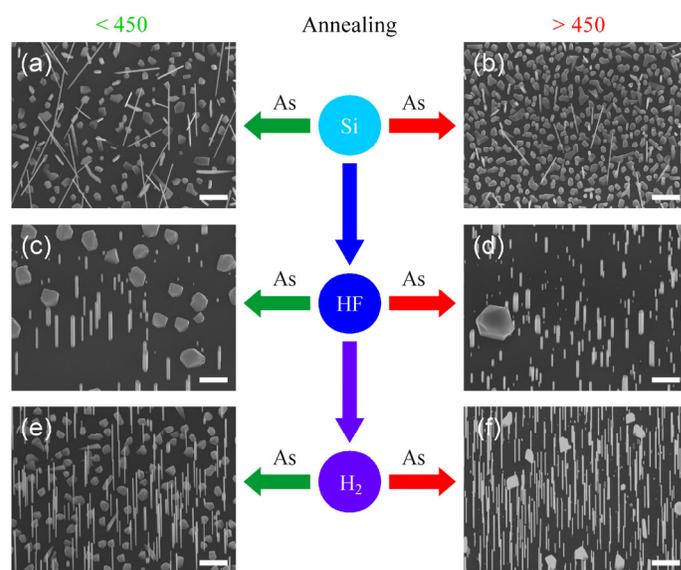
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substrates are immediately loaded into the MBE chamber. The degassing of these wafers is carried out at 200 °C for 1 h under a hydrogen flux. We use either a 1 sccm flux of hydrogen gas or a 1 sccm flux of hydrogen plasma (RF source and Power = 250 W). Atomic force microscopy (AFM) measurements performed just after this surface preparation are reported in Section S1 in the Electronic Supplementary Material (ESM) and show no noticeable evolution of the silicon roughness. Next, the substrates are loaded into the growth chamber where they are directly heated up to the growth temperature (410 °C) under an arsenic flux of  $2 \times 10^7$  Torr for 1 h. The growth temperature is optimized to limit the parasitic growth (islands and two-dimensional (2D) layer) as reported in the ESM) and to achieve high aspect ratio wires. Finally, the NW growth is initiated by opening the In shutter for 1 h. The different fluxes we used during this study are  $0.8 \times 10^{-8}$ ,  $1.5 \times 10^{-8}$  and  $3.1 \times 10^{-8}$  Torr for indium and  $1.2 \times 10^{-5}$ ,  $1.8 \times 10^{-5}$  and  $2.4 \times 10^{-5}$  Torr for arsenic. Note that an In flux of  $3.1 \times 10^{-8}$  Torr corresponds to growth rate of 0.02 monolayer/sec on GaAs and an As flux of  $2.4 \times 10^{-8}$  Torr corresponds to a growth rate of 1 monolayer/sec on GaAs. After growth, the NWs are cooled down to 200 °C using the same arsenic flux. The NWs were characterized by scanning electron microscopy (SEM, FEI Aztec-600i) and transmission electron microscopy (TEM), using a JEOL 2100F with field emission gun for high resolution analysis (HRTEM) and a JEOL Cold FEG probe-corrected ARM200F for STEM/HAADF and STEM/EDX analysis. Strain maps were calculated using the open source Strain++ program [34] based on the geometric phase analysis (GPA) algorithm by Hytch et al. [35].

### 3 Results and discussions

Figure 1 presents SEM images of samples having the same growth conditions (i.e. same arsenic flux, indium flux and growth temperature) but different surface preparations (HF etching, annealing at high or growth temperature, H<sub>2</sub> surface preparation during wafer degassing). Interestingly, and as reported before [36], the chemical etching of the native oxide with HF is mandatory to achieve growth of vertical nanowires (Figs. 1(c)–(f)); but not the high temperature annealing under arsenic flux (Figs. 1(c) and 1(e)). The opposition between these observations and the literature about MOVPE InAs NW growth [36, 37] should originate from the growth environment differences between MBE and MOVPE (H<sub>2</sub> and pressure), leading to a faster re-growth of the native oxide in a MOVPE reactor. Moreover, samples with H<sub>2</sub> preparation (Figs. 1(e) and 1(f)) have always a better aspect ratio (thinner wires) compared to other samples. This originates from different surface terminations after the H<sub>2</sub> preparation leading to different diffusion lengths of elements III on the substrate surface [27]. Consequently, crossing the BEOL temperature limit to grow fully vertical self-catalyzed InAs nanowires on silicon is not needed (Fig. 1(e)) and using a pre-growth hydrogen treatment leads to thinner wires. The H<sub>2</sub> environment during substrate degassing is expected to increase the indium diffusion length by filling dangling bonds. This could explain the differences observed between MBE and MOVPE growth of InAs NWs [22, 24, 27, 33, 38, 39] since H<sub>2</sub>, which is the carrier gas in MOVPE reactors, is lacking during MBE growth.

The structural investigation was carried out by TEM on NWs grown using the surface preparation corresponding to the NWs shown in Fig. 1(e). The crystalline structure was first analyzed by HRTEM on NWs that were mechanically transferred on a carbon holey grid. As generally observed [40], the measured InAs NWs (Sections S4 and S5 in the ESM) grow along the  $\langle 111 \rangle$  direction and are composed of a mixture of wurzite (WZ) and zinc-blende (ZB) segments. Interestingly, the bottom region exhibits a majority of ZB segments separated by several twin planes whereas the top of the NWs contains more WZ regions.

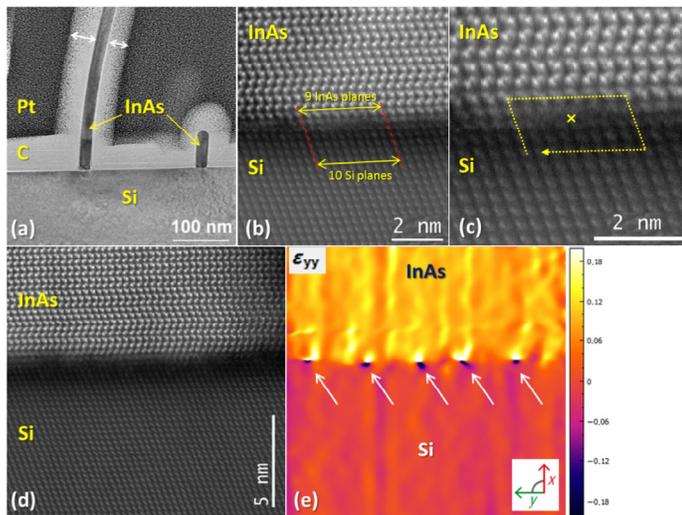


**Figure 1** Surface preparations and nanowire growths. (a)–(f) SEM images of InAs nanowires grown on silicon (111) wafers using the same growth conditions but different surface preparations. The processes are divided in two: ((a), (c) and (e)) are compatible with the BEOL limitations with an *in-situ* annealing at growth temperature whereas ((b), (d) and (f)) are annealed at higher temperature. For (a) and (b), the native oxide is present when samples are loaded into the growth chamber. For (c) and (d), the native oxide is removed using an HF 5% solution for 1 min prior to the loading into the MBE reactor. For (e) and (f), a flux of hydrogen is used during the sample degassing (after the native oxide removal). The scale bars correspond to 500 nm.

Subsequently, cross-section specimens with InAs NWs still attached to the Si substrate were prepared by Focused Ion Beam (FIB). This made it possible to take STEM/HAADF images at the interface between InAs NWs and the Si substrate, so to clearly identify the InAs NWs surface as B-type (i.e. As-terminated, cf. Fig. S3(d) in the ESM). Additional information about the crystalline quality of the Si/InAs interface was gained from the FIB-prepared cross-section specimens. To this purpose, NWs need to be coated with evaporated carbon prior to FIB preparation.

However, as shown in Fig. 2(a), non-uniformity in the carbon deposition on each side of the NWs (cf. white arrows) may result in stress-induced bending of the NWs, which is clearly visible in the case of long NWs (cf. NW on the left-hand side of Fig. 2(a)). In the case of long NWs ( $\sim 2 \mu\text{m}$ ), the induced stress can even exceed the plastic deformation threshold ( $\sim 5 \text{ GPa}$  for traction fracture in InAs NWs [41, 42]) and dislocations are therefore formed close to the InAs/Si interface (Section S4 in the ESM).

The interface analysis was therefore performed on small NWs (length  $< 100 \text{ nm}$ ) where bending effects are negligible (Fig. 2(a)). A typical image of the InAs/Si interface region, obtained by STEM/HAADF is shown in Fig. 2(b). The InAs and Si layers are perfectly aligned and are separated by a weak contrast band corresponding to the native SiO<sub>2</sub> layer which covers the Si surface around the NW (as schematically shown in Section S5 in the ESM). Such layer weakens the image contrast but does not stop the atomic planes to be visible throughout the interface in STEM/HAADF images (Figs. 2(b)–(2(d))), clearly indicating that InAs growth occurs epitaxially on the Si substrate. In addition, along the direction parallel to the interface, about 9 InAs(111) planes are observed for every 10 corresponding Si(111) planes (Fig. 2(b)), in agreement with the difference in the lattice constant of ZB InAs ( $6.058 \text{ \AA}$ ) with respect to Si ( $a_{\text{Si}}/a_{\text{InAs}} = 0.897$ ). The InAs NWs can therefore be considered as fully relaxed and misfit dislocations are expected to form, as enlightened by the Burgers circuit in Fig. 2(c) (showing an isolated misfit dislocation) or by the geometrical phase analysis (GPA) method applied to a

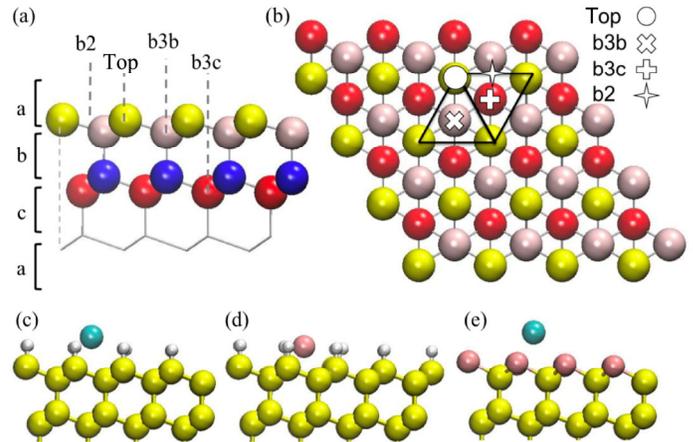


**Figure 2** (a) Cross-section TEM image of InAs NWs still attached to the Si(111) substrate. Non-uniformity in the carbon deposition on each side of the NWs (cf. white arrows) may result in stress-induced bending of long NWs (cf. NW on the left of the image). (b)–(d) STEM/HAADF images taken at the interface between an InAs NW and the Si substrate indicating that the InAs growth occurs epitaxially on the Si substrate. The weak contrast band located at the InAs/Si interface corresponds to the native SiO<sub>2</sub> layer covering the Si surface around the NW (cf. Section S3 in the ESM). (b) Along the direction parallel to the interface, about 9 InAs(111) planes are observed for every 10 corresponding Si(111) planes, in agreement with the ratio between the lattice constants of InAs and Si ( $a[\text{Si}]/a[\text{InAs}] = 0.897$ ). The InAs NWs can therefore be considered as fully relaxed. (c) A Burgers circuit drawn at the InAs/Si interface allows to identify the position of an isolated misfit dislocation. (d) STEM/HAADF image of the InAs/Si interface region and (e) corresponding strain mapping ( $\epsilon_{yy}$ ) in the direction parallel to the interface obtained by GPA. Five dislocations are visible within a distance of  $\sim 11$  nm along the interface, in agreement with a complete relaxation of the InAs lattice.

lower magnification image (Figs. 2(d) and 2(e)). In this case, five dislocations are observed within a distance of  $\sim 11$  nm along the interface, again in agreement with a complete relaxation of the InAs lattice. Consequently, the proposed surface preparation (Fig. 1(e)) leads to the fully relaxed epitaxial growth of InAs NWs on silicon respecting a 410 °C thermal budget.

In order to understand the role of hydrogen and arsenic on the Si(111) surface during NWs nucleation, we performed density functional theory (DFT) calculations as reported in Fig. 3. In these simulations, we model the Si(111) surface using a  $(4 \times 4)$  simulation cell (details of calculations are given in Section S6 in the ESM). Two different surface terminations depending on the surface treatments are considered (Section S7 in the ESM). From literature, we know that HF etching and degassing leave the surface mainly covered with hydrogen [43], so an H-terminated Si(111): $1 \times 1$  surface is considered, where H atoms fill the dangling bonds of the topmost silicon layer (Fig. S7(b) in the ESM). Considering the *in-situ* arsenic preparation, an As layer substituting to the topmost layer of Si substrate was used, commonly referred as the As-terminated Si(111): $1 \times 1$  reconstruction (Fig. S7(c) in the ESM). Such surface has already been studied in detail experimentally [44–46] revealing that an As-terminated Si(111): $1 \times 1$  prevents the Si  $7 \times 7$  reconstruction. *Ab-initio* calculations about the precise As position with respect to the silicon matrix have already been performed [47, 48] fitting with our model (Si-As bond length of 2.46 Å). It is worth noting that this structure is so stable that it is often considered as an effective passivation of the silicon surface. Other surfaces were investigated and appeared not to be relevant for this study (comments given in Section S7 in the ESM).

The adsorption of both In and As atoms, also called ad-atoms in the following, on H-terminated Si(111): $1 \times 1$  have been performed



**Figure 3** DFT calculations. (a) Side view and (b) top view of the Si(111) slab used in the calculations where the investigated adsorption sites are shown: top, b2, b3b, b3c. The first to fourth layers are colored in yellow, beige, blue and red, respectively in order to highlight repeating pattern observed in the layers stacking of (111) oriented Si crystal. (c) Adsorbed configurations of In on H-terminated Si(111): $1 \times 1$  surface as resulted from HF treated surface. (d) Adsorbed configurations of As on H-terminated Si(111): $1 \times 1$  surface. (e) Adsorbed configurations of In on As-terminated Si(111): $1 \times 1$  surface after an arsenic treatment. In (c), (d) and (e), yellow, white, cyan and pink spheres are respectively Si, H, In and As atoms. This color scheme is also used in Section S4 in the ESM.

likewise the adsorption of In ad-atom on As-terminated Si(111): $1 \times 1$ . Several initial positions for the ad-atoms have been tested as a function of the Si(111) topology and, taking advantages of the symmetry of the system, only the most favorable configurations are discussed in the following. The top configuration corresponds to an ad-atom adsorbed above one atom of the topmost layer (either H or As atom as a function of the surface treatment). Two other configurations are discussed, where As or In atom can adsorb as a bridge configuration either between two atoms of the topmost layer (As or H species) referred as b2 adsorption site or between three atoms of the topmost layer, either As or H specie, and named b3b and b3c depending on the layer stacking of the silicon Si(111) substrate as schematized in Figs. 3(a) and 3(b) (with respect to the periodic abc-like stacking in the Si(111) substrate). Thus, the hydrogen preparation of the surfaces, prior to growth, not only fills all dangling bonds, increasing the diffusion of elements III, but also prevents indium and arsenic incorporation at low temperature. Keeping “clean” surfaces, hydrogen allows to reduce the annealing temperature at which is formed the As-term Si surface.

Adsorption energies (see Fig. S8 in the ESM) and typical bond lengths are provided in Table 1. For the adsorption of As and In atoms on H-terminated surface, the adsorption energies are endothermic or slightly exothermic for the most favored adsorptions ( $-0.85$  eV for In adsorption Fig. 3(c)). Note here that the adsorption of As ad-atom implies a deep deformation in the H atoms layer where H atoms are repelled from As atom to allow the ad-atom As to come closer to the underlying topmost layers of the Si substrate, revealing a favorable interaction between Si and As species (Fig. 3(d)). Such a deformation of the whole system involves a significant deformation cost as revealed by the energetic penalty of the adsorption energy. These observations are consistent with the measured typical bond lengths on such adsorbed states which are larger than the ones from references calculations on simple molecules (like InH<sub>3</sub> and AsH<sub>3</sub>) and from tabulated experimental data. Thus, the H atoms prefer to maintain a strong bond with the Si substrate and keep the ad-atoms far from the surface. To go further, we perform calculations to evaluate if In atom can adsorb on H-terminated Si(111): $1 \times 1$  through more complex mechanisms involving H<sub>2</sub> or InH<sub>3</sub> desorption. Only the desorption of an InH<sub>3</sub> molecule associated to the subsequent

**Table 1** Adsorption energy ( $E_{ads}$  in eV) and typical bondlength ( $d$  in Å) for single As and In on H-term surface and Adsorption energy for single In on As-term surface

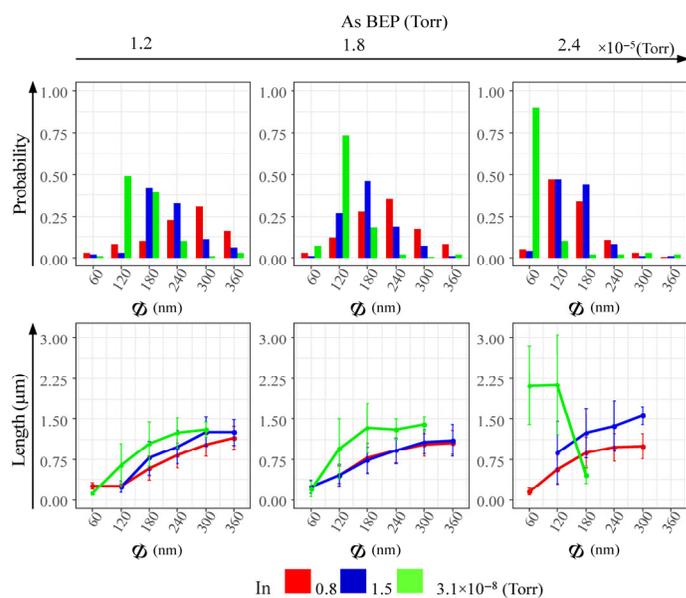
	H-terminated Si(111):1 × 1		As-terminated Si(111):1 × 1		As-terminated Si(111):1 × 1	
	As adsorption		In adsorption		In adsorption	
	$E_{ads}$ (eV)	$d(As-H)$ (Å)	$E_{ads}$ (eV)	$d(In-H)$ (Å)	$E_{ads}$ (eV)	$d(In-As)$ (Å)
Top					-1.24	2.88
b2	-0.41	2.12	-0.83	2.55	Non stable	—
b3b	0.73	2.70	-0.83	2.54	-1.58	3.15
b3c	0.33	2.70	-0.85	2.54	-1.60	3.17

adsorption of an In atom on the empty space “b3 site” left is a favorable exothermic process. Considering energetics of Table 1, such mechanism involving Si-H breaking must require a thermal activation. Investigating such reaction paths and associated activation barriers is beyond the scope of this study. This confirms that the adsorption reaction of both As and In on H-terminated surface is not favorable at low temperature.

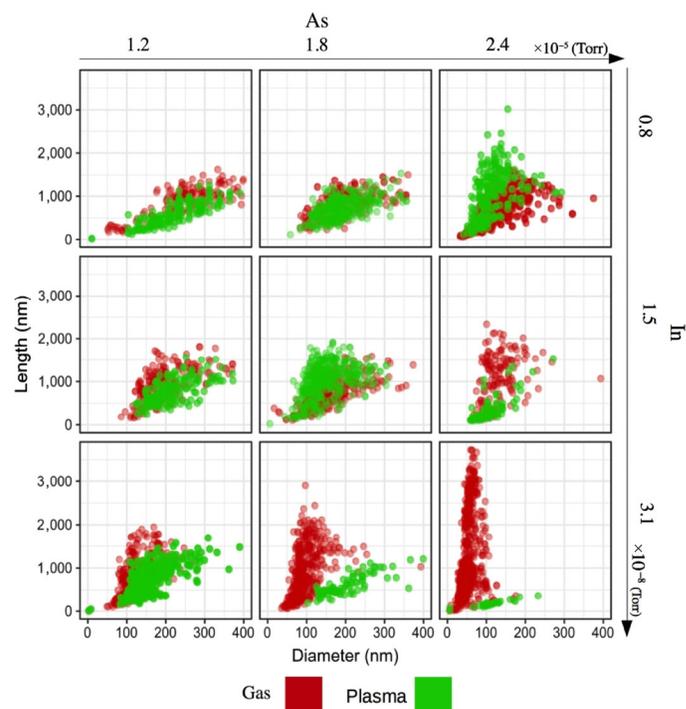
In addition, in the case of the adsorption of In atom on As-terminated Si surface, large adsorption energies are observed favoring b3-type sites. Top configuration is also an observed adsorbed state which reveals to be metastable reaching b3-type configurations without any activation barrier (Fig. 3(e)). DFT calculations highlight the favorable adsorption of In species on As-terminated Si(111):1 × 1, which is stabilized at the early stages of deposition as a bridge configuration. We also estimate the barrier energy for the adsorbed In atom on a b3 site to reach a nearby b3 site using NEB calculations. A very low activation barrier of 0.10 eV was obtained (or 0.35 eV when passing by top configuration), highlighting the ability of the In atom to migrate on the surface, which is favorable for the nucleation process.

In order to characterize the influence of the hydrogen preparation on the InAs NW growth, a complete growth study was performed using the Fig. 1(e) surface preparation as a starting point. Here, all samples are degassed at 200 °C for 1 h under a hydrogen gas flux, and an *in-situ* annealing under arsenic for 1 h is performed in the growth chamber and at growth temperature (~ 410 °C). From each sample, more than 150 NWs were characterized using the method described in Sections S9 and S10 in the ESM. Creating families of homogeneous diameters (the  $x$  axis of each graph in Fig. 4), it is possible to perform statistics and plot the length and the percentage of each family for different indium and arsenic fluxes as reported in Fig. 4. As already reported in Ref. [15], the NW diameter decreases when the arsenic flux is increased (see the probability part of Fig. 4), whatever the indium flux is. This is consistent with other MBE study about InAs NW growth [20] and a self-catalyzed growth mechanism (vapor solid (VS) growth mechanism). Interestingly, when the indium and arsenic fluxes are both increased simultaneously ( $3.1 \times 10^{-8}$  Torr for In and  $2.4 \times 10^{-5}$  Torr for As), long and thin NWs can be obtained. This “abnormal” behavior is the consequence of a change in the growth mechanism from VS to vapor liquid solid (VLS) as already reported for InP NWs [49]. Obtaining “clean” substrate surfaces thanks to the hydrogen preparation and optimizing the growth conditions, makes it possible to maximize the aspect ratio of VLS InAs NWs on silicon.

Finally, in order to assess the differences between H<sub>2</sub>-gas and H<sub>2</sub>-plasma treatments, all the growth conditions investigated in Fig. 4 have been repeated in the case of the H<sub>2</sub>-plasma preparation. Using the same procedure (Sections S9 and S10 in the ESM), more than 150 NWs are measured for each sample resulting in statistics reported in Fig. 5. In this plot, we clearly see that NWs grown from H<sub>2</sub>-gas (Red) and H<sub>2</sub>-plasma (Green) surfaces are different when increasing the arsenic and indium fluxes. Although the H<sub>2</sub>-gas and



**Figure 4** Statistic plots for the H<sub>2</sub>-gas treated surfaces corresponding to the Fig. 1(e) process. Nanowires are grouped in families of different diameters (see Sections S7 and S8 in the ESM). The three colors (red, blue, green) correspond to different indium fluxes. On top, the proportion of each family is reported as a function of the arsenic flux. On bottom, the mean length of each family is reported as a function of the arsenic flux. These statistics graphs allow to evaluate the influence of the indium and arsenic fluxes on the diameter and the length of the InAs nanowires.



**Figure 5** Comparisons between the H<sub>2</sub>-gas (in red) and H<sub>2</sub>-plasma (in green) surface preparations. Each of the 9 scatter plots correspond to one specific growth condition associated with the arsenic and indium fluxes reported on top and on right. For each plot, the  $x$ -axis corresponds to the diameter and the  $y$ -axis to length of the nanowires. Each point represents a unique nanowire measured either for the H<sub>2</sub>-gas (in red) or the H<sub>2</sub>-plasma (in green) surface preparations (Fig. 1(e)). Red and green points are almost superimposable for low indium and arsenic fluxes but are well separated for high indium and arsenic fluxes.

H<sub>2</sub>-plasma preparations are not expected to give dramatically different surfaces, major changes are observed. While H<sub>2</sub>-gas treated surfaces favor long and thin wires when indium and arsenic fluxes are

increased, the opposite is observed for H<sub>2</sub>-plasma treated surfaces. This could be explained by a filling of the dangling bonds and a smoother surface for the H<sub>2</sub>-gas preparation in opposition with the H<sub>2</sub>-plasma one. Indeed, the element III diffusion length appears to increase for a H<sub>2</sub>-gas prepared surface leading to a change of the growth mechanism from VS to VLS.

## 4 Conclusions

To conclude, we propose a process allowing the growth of fully vertical InAs NWs on Si by MBE without crossing the 410 °C growth temperature, which is compatible with the BEOL limitations. The “key” role of hydrogen during substrate preparation is presented and discussed in details from both experimental and theoretical point of view. A description of the different surface preparations is proposed and consequences on the NW growth are presented. The change from a VS to a VLS growth mechanism for self-catalyzed InAs NWs is reported and explained by surface diffusion of element III. Our results further explain the differences observed between MBE and MOVPE growth of InAs NWs on silicon leading to a better understanding of the nucleation mechanisms and the development of new processes involving hydrogen preparations. Finally, an unexpected difference between H<sub>2</sub>-gas and H<sub>2</sub>-plasma surface preparations is reported and related to surface termination.

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**Electronic Supplementary Material:** Supplementary material (additional information about insight of surface treatments for CMOS compatibility of InAs nanowires) is available in the online version of this article at <https://doi.org/10.1007/s12274-2257-8>.

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