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Towards high mobility InSb nanowire devices

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Abstract

We study the low-temperature electron mobility of InSb nanowires. We extract the mobility at 4.2 K by means of field effect transport measurements using a model consisting of a nanowire-transistor with contact resistances. This model enables an accurate extraction of device parameters, thereby allowing for a systematic study of the nanowire mobility. We identify factors affecting the mobility, and after optimization obtain a field effect mobility of $\sim 2.5 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. We further demonstrate the reproducibility of these mobility values which are among the highest reported for nanowires. Our investigations indicate that the mobility is currently limited by adsorption of molecules to the nanowire surface and/or the substrate.

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Keywords: field effect mobility, adsorption, nanowire transistor, nanowire FET, nanofabrication

(Some figures may appear in colour only in the online journal)

1. Introduction

Advances in nanowire growth have led to development of novel quantum devices, such as Cooper-pair splitters [1], hybrid semiconductor–superconductor devices [2] and spin–orbit qubits [3]. Nanowire devices thus allow exploration of mesoscopic transport in a highly confined system and show potential as a quantum computation platform. Outstanding nanowire transport properties, such as a high level of tunability of device conductance and low disorder, have been essential to the realization of these experiments.

Recently, hybrid superconductor–semiconducting nanowire devices have been identified [4, 5] as a suitable platform to study Majorana end modes [6], zero-energy bound states that exhibit topological properties. Among various systems, InSb nanowires emerged as a very promising candidate due to their

large spin–orbit interaction and large g factor. Reports on signatures of Majorana bound states in InSb nanowire-based systems followed quickly after their theoretical prediction [7–9]. To further develop this topological system, a reduction of the disorder in the nanowire is essential [10, 11]. Disorder reduces or even closes the topological gap that gives Majoranas their robustness, thereby impairing their use as topological qubits. Disorder is quantified by measurements of carrier mobility, which relates directly to the time between scattering events. Evaluation of carrier mobility in nanowires therefore indicates their potential for transport experiments and is thus crucial to further development of nanowire-based quantum devices.

According to the Matthiessen rule, various scattering mechanisms altogether determine the net mobility through [12]

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \dots \quad (1)$$

⁴ Equal contribution.

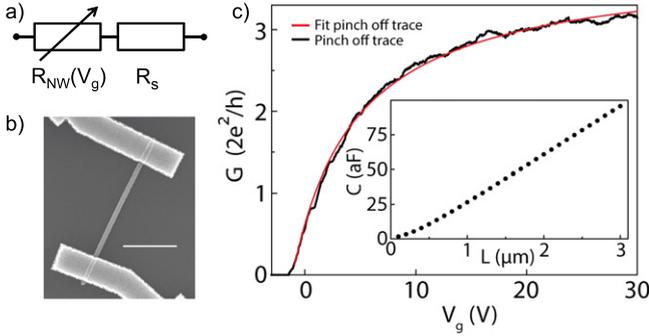


Figure 1. (a) Electrical diagram of the InSb nanowire FET. The FET is modelled as a nanowire channel with a resistance controlled by a nearby gate, $R_{NW}(V_g) = G_{NW}^{-1}(V_g)$, in series with fixed interface resistances, R_s . (b) Electron microscope image of an InSb nanowire FET. Nanowire diameter is ~ 100 nm. The nanowire is deposited onto a Si substrate covered with 285 nm dry thermal SiO_2 . Ti/Au (5/145 nm) contacts have spacing of 1, 1.5, 2 or 2.5 μm . Scale bar is 1 μm . (c) Conductance G , as a function of back gate voltage V_g (black curve). Source–drain bias is set to 10 mV throughout the study. Field effect mobility is extracted from a fit to the conductance (red curve) using equation (3). All measurements are performed at a temperature of 4.2 K. Inset: gate–nanowire capacitance C , as a function of source–drain contact spacing L . Capacitance is extracted from a finite element model of the device geometry. Contacts are included in the simulated device geometry and lead to a nonlinear $C(L)$ at small contact spacing.

Here μ represents the net mobility which results from distinct scattering mechanisms each giving rise to a separate mobility μ_n . In other words, the most dominant scattering contribution limits and hence determines the net mobility. Therefore the mobility can be improved by identifying the limiting mechanism and subsequently reducing or eliminating it.

Apart from the recently introduced Hall effect measurements on nanowires [13, 14], field effect transport measurements are the most common and experimentally most feasible method to extract charge carrier mobility in these systems. Here, one measures the current flowing through the nanowire channel contacted by two electrodes as a function of the gate voltage with fixed voltage bias. The conductance of the channel is described by the linear region of the accumulation regime of a field effect transistor (FET) [15]. In this case the conductance of the channel is

$$G(V_g) = \frac{\mu C}{L^2}(V_g - V_{th}), \quad (2)$$

with gate voltage, V_g , mobility, μ , capacitance, C , channel length, L , and threshold voltage, V_{th} . If the capacitance and the channel length are known, the field effect mobility can be determined from the transconductance, $g_m = dG/dV_g$. In most cases, to extract the mobility, the maximum (peak) transconductance is used. One should note that both the mobility and the field effect transport is described using the Drude model where charge carrier transport is classical and diffusive.

Previous studies showed that low-temperature field effect mobility for nominally undoped III–V nanowires is mainly limited by crystal defects such as stacking faults [16–20], and surface effects such as surface roughness [21, 22]. Point

defects are also thought to have an effect on the mobility [23]. However, as they are difficult to detect so far no direct connection between impurities and mobility has been reported. Highest reported low-temperature field effect mobilities are $1.6\text{--}2.5 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Such mobilities are observed in InAs nanowires [16, 24], InAs/InP core–shell nanowires [25, 26] and GaN/AlN/AlGaIn core–shell nanowires after correction for contact resistances [27]. However, in most of these studies either data on a single device is reported, or the average mobility of several devices is significantly lower than the reported maximum [26]. Systematic studies of such high-mobility nanowire FETs are thus largely lacking.

Concerning field effect mobility, the InSb nanowires we investigate differ in several respects from their oft-studied InAs counterparts: the InSb nanowires we use have a larger diameter of approximately 100 nm, reducing their surface-to-volume ratio compared to the thinner InAs nanowires, and are likely to have no surface accumulation layer. Instead, upward band bending leading to surface carrier depletion has been reported for both clean [28] and oxygen-covered InSb surfaces with (110) orientation, the orientation of our InSb nanowire facets. As the InSb facets are atomically flat no surface roughness is expected. Finally, the nanowires are purely zinc-blende and are free of stacking faults and dislocations. The growth of InSb nanowires we study is described in [29] and [30]. Given the differences between InSb nanowires and other nanowire materials it is an open question what determines the low-temperature mobility in InSb nanowires. We note that while in [29] field effect mobilities of these InSb wires are reported, no systematic investigation of the nanowire mobility was performed. The mobility extraction method presented here allows such a thorough investigation, thereby revealing new insights on nanowire mobility.

To identify the factors affecting the mobility of InSb nanowires, we characterized the low-temperature mobility of nanowire FETs fabricated using different experimental parameters. We tailored the extraction of field effect mobility for the nanowires we study to accurately determine the essential transistor parameters of nanowire FETs. By systematic studies we developed a recipe that results in reproducible average mobilities of $\sim 2.5 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. While this value represents an average over many devices, the extracted mobility from a single measurement may exceed $3.5 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. After optimizing the fabrication, we also find that adhesion of molecules to the nanowire and/or the substrate currently limits the extracted mobility. Although such adsorption effects are known to modify the nanowire conductance [17, 31] and also the room-temperature mobility [32–34] (note that [33] reports an increase of mobility upon adsorption, whereas [34] a reduction), our identification of surface adsorption being the limiting factor to low-temperature field effect mobility is new. The amount of adsorbate is reduced by evacuating the sample space for longer time prior to cool down and suggestions for further reduction of the adsorbates as well as to minimize their contribution to the field effect transport are made. We finally discuss various

methods to investigate the surface properties of InSb nanowires.

2. Experimental details

InSb nanowire FETs are fabricated on a heavily doped Si substrate (used as a global back-gate) terminated with a 285 nm thick dry thermal SiO₂ (figure 1(b)). The substrate is patterned with alignment markers prior to nanowire deposition. Nanowires are positioned on the substrate using a micro-manipulator [35]. Two terminal contacts are realized by electron beam lithography, metal evaporation (Ti/Au 5/145 nm) and lift-off. Argon plasma etching is employed prior to contact deposition. Further details about the fabrication process and the measurements can be found in supplementary text 1 and 2, respectively.

Due to the absence of a surface accumulation layer in InSb nanowires, an interface resistance of a few kilo ohms cannot be eliminated upon contacting the nanowire [36]. Such interface resistances are known to reduce the transconductance, resulting in an underestimation of the intrinsic mobility [37, 38]. Moreover, at a temperature of 4 K universal conductance fluctuations complicate the extraction of mobility from transconductance. We therefore tailor the extraction of field effect mobility to our InSb nanowire FETs [39]. We model the interface resistances by a resistor R_s with a fixed value (no gate voltage dependence), connected in series to the nanowire channel. A substantial part of the device resistance at high gate voltage stems from the interface resistances, strongly affecting the gate voltage dependent conductance. This complicates accounting for a possible change of mobility with gate voltage. We therefore assume a mobility independent of gate voltage. The device conductance is then given by (see also figure 1(a))

$$G(V_g) = \left(R_s + \frac{L^2}{\mu C (V_g - V_{th})} \right)^{-1}. \quad (3)$$

This equation allows for extraction of field effect mobility using a fit to the measured $G(V_g)$. Here, the mobility μ , the interface resistances R_s , and the threshold voltage V_{th} are the free fit parameters. We restrict the fitting range to $G^{-1}(V_g) \leq 100$ k Ω . We independently calculate the capacitance from a finite element model of the device (see figure 1(c) inset), where we take into account that quantum confinement in our nanowires reduces the classical capacitance by $\sim 20\%$ [40, 41]. Neglecting quantum effects in our capacitance calculation would lower the extracted mobility values by $\sim 20\%$. Further details on the calculation of the capacitance can be found in supplementary text 3. We compared the mobility values extracted by a fit using equation (3) with the mobility values obtained from peak transconductance, a common method to extract nanowire mobility, and found matching results (see supplementary text 4). For a representative fabrication run, mean forward mobility of 11 devices is found to be 2.9×10^4 cm² V⁻¹ s⁻¹ using our fit method,

whereas peak-transconductance method yields $2.7 (1.9) \times 10^4$ cm² V⁻¹ s⁻¹ with (without) taking into account the interface resistances. Our fit method, however, differs from peak transconductance method where the mobility is extracted from the maximum value of the transconductance using a small gate voltage range. Because we consider the transconductance in a wide gate voltage range by fitting a large section of $G(V_g)$, the extracted mobility is insensitive to small conductance fluctuations. This is contrary to the peak transconductance where conductance fluctuations greatly affect the extracted mobility. We show in supplementary text 5 that our simple model with gate voltage-independent interface resistances is a valid approximation for our measurements. However, despite our thorough analysis a general drawback of field effect mobility remains: the uncertainty in the calculated capacitance value affects the extracted mobility directly. Nanowires suffer from this drawback as their small dimensions do not allow a straightforward experimental extraction of capacitance.

To determine what limits the mobility in our devices, we systematically studied the effect of various experimental parameters by measuring ~ 10 devices simultaneously fabricated on the same substrate. We then change one parameter at a time for each fabrication run to deduce its effect on the field effect mobility.

3. Results and discussions

3.1. Nanowire surface and adsorption

Nanowire conductivity at room temperature is known to increase after evacuation of the sample space following mounting of devices [17, 42]. We find that evacuation also strongly affects $G(V_g)$ at low temperature (4 K). Comparing the $G(V_g)$ measured for short and long sample space evacuation time prior to cool down, we observe a steeper increase of conductance with gate voltage after long-time evacuation (figure 2(a)). Considering a number of devices on the same measurement chip, we find almost a doubling of the mobility values after long-time sample evacuation (figure 2(b)). The re-exposure of samples to air after long-time evacuation results in a reduction of mobility (figure 2(c)) with values very similar to those obtained from the initial measurements with a short-time sample space evacuation. The transconductance is larger when the gate is swept from low towards high voltages (forward sweep direction) leading to higher mobility compared to the case of sweeping from high gate voltages to low (reverse sweep direction) (figure 2(c)). Moreover, after long-time evacuation a shift of the threshold voltage towards more negative values is observed (figure 2(d)) together with a reduced hysteresis (figure 2(e)). Both the threshold voltage and the hysteresis regain their initial values obtained from short-time evacuation once the sample is re-exposed to air, similar to the extracted mobility: exposing the devices to air has a reversible effect on the field effect transport parameters we extract from the fits. All

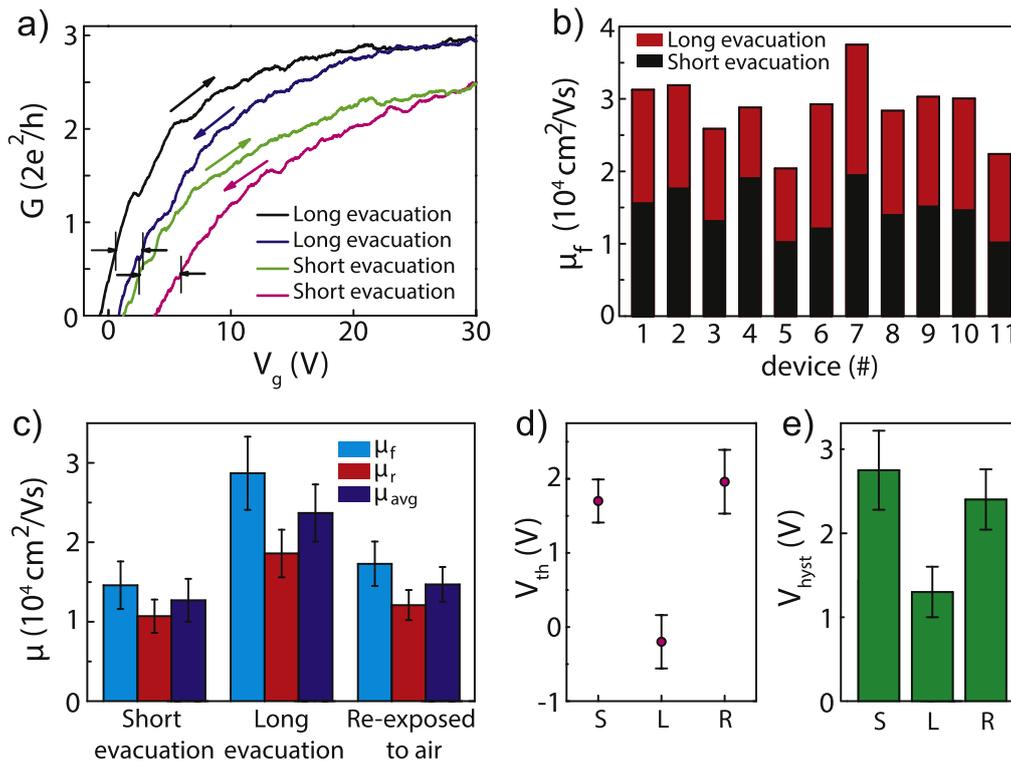


Figure 2. (a) Conductance $G(V_g)$ of samples measured after evacuation of the sample space for a short or long period of time prior to cool down. Samples are evacuated for ~ 15 min (~ 65 h), giving the green and pink (black and blue) conductance curves for forward and reverse sweep direction respectively. Arrows indicate sweep direction. The same chip with nanowire devices is first evacuated only shortly (yielding the data denoted with ‘short evacuation’), then evacuated for longer-time (‘long evacuation’ data), reexposed to air for ~ 90 h and evacuated shortly (~ 15 min) again (‘re-exposure’ data), see panel (c). The substrate was cleaned prior to nanowire deposition. Hysteresis of both pairs of conductance curves is indicated with arrows and vertical lines. Although the hysteresis is indicated at non-zero G , the hysteresis reported in panel (c) is extracted from the difference in threshold voltage between conductance curves with forward and reverse sweep direction. (b) Mobility obtained with forward sweep direction, μ_f , of individual devices after short (black) or long (red) device evacuation time. (c) Mobility after short-time evacuation, long-time evacuation, and re-exposure to air. μ_{avg} is the average of the mobility obtained with forward sweep direction, μ_f , and with reverse sweep direction, μ_r . (d) Threshold voltage extracted from forward sweep direction, V_{th} after short-time evacuation (S), long-time evacuation (L) and re-exposure to air (R). (e) Hysteresis V_{hyst} , after short-time evacuation (S), long-time evacuation (L) and re-exposure to air (R). The hysteresis is given by the difference in threshold voltage between forward and reverse sweep direction. All values in panels (c)–(e) are an average, obtained from fits to the conductance curve of each device on the measurement chip. Error bars in panels (c)–(e) indicate the standard deviation.

extracted fit parameters can be found in supplementary table 1.

A hysteresis in transconductance dependent on ambient conditions has been studied before by Kim *et al* [43] and Wang *et al* [44], and was attributed to the adsorption of water onto the nanostructure and onto the SiO_2 substrate. Evacuation of the sample environment leads to desorption of water, thereby reducing the hysteresis. However sample evacuation alone is insufficient to fully remove the adsorbed water. The similarities between our observations and those reported by Wang *et al* and Kim *et al*, considering both the influence of gate voltage sweep direction on the shift of the threshold voltage, as well as the reduction of hysteresis with evacuation time and the reversibility of the effect when reexposing samples to air, strongly suggest that the field effect transport is affected by molecules adsorbed to the nanowire and/or the SiO_2 substrate. Water is highly likely to be the main adsorbate because reexposing the device to ambient atmosphere

following long evacuation time of sample space yields values of mobility, threshold voltage and hysteresis similar to those obtained from the measurements with short evacuation time. InSb nanowires have however also shown decreased conductance in response to isopropanol and acetone [31].

It is an open question how adsorbates affect device conductance at low temperature. The alignment of polar molecules by gate electric field may result in an additional gating [44]. However, the mechanism through which such alignment causes hysteresis is not clear. Another scenario is charge trapping by adsorbed molecules [43]. Such trapping could possibly lead to an asymmetry between forward and reverse sweep direction, yielding the observed hysteresis and sweep direction dependent mobility. The observed trapping mechanism is likely to have a long response time, as our measurements are taken at relatively low gate voltage sweep rates (120 mV s^{-1}). Unlike [32, 43, 44], we find no dependence on sweep rate for rates between 3 and 600 mV s^{-1} .

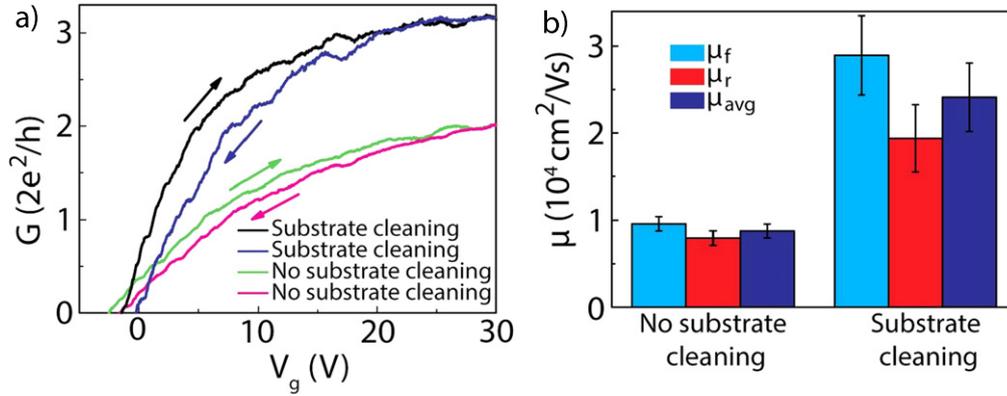


Figure 3. (a) Conductance curves $G(V_g)$ obtained from samples without and with substrate cleaning. Forward and reverse sweep direction are indicated with arrows. Samples have been evacuated for ~ 60 h before cool down. (b) Forward, reverse and average mobility with and without substrate cleaning. Values are averages obtained from fits to conductance curves of individual devices. Error bars indicate standard deviation.

Nonetheless, repeated measurements yield the same $G(V_g)$, implying that between scans the traps are emptied.

3.2. Substrate cleaning

We further find that cleaning of Si/SiO₂ substrates by remote oxygen plasma prior to nanowire deposition results in an enhanced gate dependence of low-temperature conductivity. Figure 3(a) shows $G(V_g)$ curves of individual devices, while figure 3(b) shows an average over extracted mobilities obtained from measurements of ~ 10 FETs with and without substrate cleaning. All other fabrication and measurement steps are the same for both sets of devices. The remote oxygen plasma most probably removes hydrocarbons that remain on the substrates after fabrication of alignment markers or during storage of samples in a polymer-containing environment. We verified that the oxygen plasma cleaning does not decrease the thickness of the SiO₂ gate dielectric within the measurable range < 1 nm.

3.3. Contact spacing

A correlation between FET source–drain contact spacing and extracted field effect mobility is found (figure 4). Although the spread in mobility at a given contact spacing is substantial, an overall increase of extracted mobility is observed with increasing contact spacing. To determine whether the dependence of the field effect mobility on contact spacing originates from the length of the used nanowire, FETs with short ($1 \mu\text{m}$) contact spacing were realized both on short wires, and on long wires using three contact electrodes resulting in two FETs in series. Devices made from both long and short wires with $1 \mu\text{m}$ contact spacing give similar mobility (see figure 4). The contact spacing dependence is thus a device property rather than a nanowire property.

A reduced mobility for short contact spacing is expected when transport is (quasi-)ballistic rather than diffusive [45, 46]. We have observed ballistic transport in our wires [36] with a device geometry and measurement conditions different from those here. Here we expect quasi-ballistic

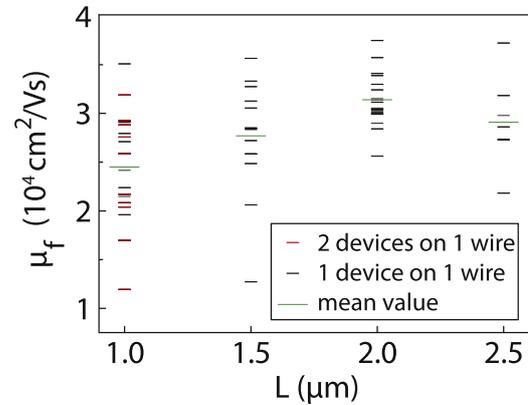


Figure 4. Mobility obtained by sweeping the gate voltage in forward direction, μ_f , as a function of source–drain contact spacing L . Data from 5 different measurement chips (see supplementary text 6). Red lines indicate mobility values obtained from long nanowires on which three contact electrodes were placed, resulting in two FETs in series, while black lines correspond to the mobility of single FET devices. Mean forward mobility for each contact spacing is $\mu_{f,m}(L = 1 \mu\text{m}) = 2.4 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, $\mu_{f,m}(L = 1.5 \mu\text{m}) = 2.8 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, $\mu_{f,m}(L = 2 \mu\text{m}) = 3.1 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $\mu_{f,m}(L = 2.5 \mu\text{m}) = 2.9 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

transport in our devices with a mean free path comparable to nanowire diameter $l_e \sim 0.1 \mu\text{m}$. While devices with $L/l_e \gg 1$ are preferable, our InSb nanowires can currently not be grown longer than $\sim 3.5 \mu\text{m}$. However, while for channel length of $1 \mu\text{m}$ (quasi-)ballistic effects may play a role, mobility values obtained from our devices with longer contact spacing yield a better estimate of field effect mobility. Moreover, effects related to the metal contacts are expected to play a larger role in devices with short contact spacing and can possibly contribute to the observed decrease of $\mu(L)$ in short channel devices. Possible explanations are that (1) the contacts reduce the capacitance of short devices more than expected from the Laplace simulations (in which the nanowire is assumed to be

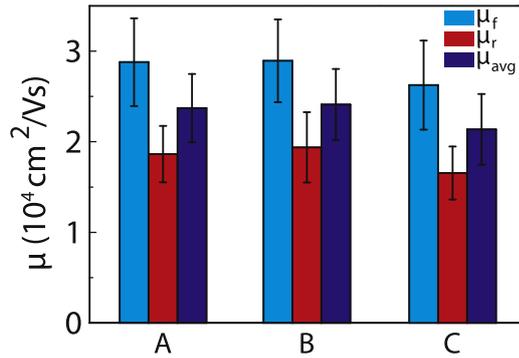


Figure 5. Average mobilities obtained with forward (μ_f) and reverse (μ_r) sweep direction. First group of data (batch A) corresponds to the fabrication run presented in figure 2 (long-time evacuation), batch B is presented in figure 3(b) (with substrate cleaning), whereas batch C is a separate batch to demonstrate the reproducibility of our results. Average mobility μ_{avg} is the average of forward and reverse mobility. All results are obtained by improved cleaning of the substrate and long evacuation time of the sample space. Error bars indicate standard deviation.

metallic) or (2) electrons are injected from and absorbed over a finite length underneath the contacts, leading to an effective L larger than the contact spacing.

3.4. Reproducibility

Altogether, cleaning the SiO_2 substrate before wire deposition and applying a long sample evacuation time yields $\mu_{\text{avg}} \approx 2.5 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for devices with a contact spacing $L = 2 \mu\text{m}$. This mobility is the average value of $\mu_f = 3.1 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ (see figure 4) and $\mu_r = 1.9 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. These high mobilities result from measurements of ~ 15 devices fabricated in different fabrication runs (see supplementary text 6 for details) using the same fabrication recipe. Figure 5 demonstrates the reproducibility of our results: mobility obtained from three different fabrication runs are very similar. The optimized nanofabrication recipe as well as an overview of all the parameters extracted from the fits to the conductance vs. gate voltage curves that yield figure 5 are given in supplementary text 1 and supplementary table 2, respectively.

4. Conclusions and outlook

Low-temperature field effect mobility of InSb nanowires is extracted by measuring the conductance as a function of gate voltage. Taking surface adsorption and substrate cleaning into consideration, an optimized nanofabrication recipe has been obtained yielding average field effect mobilities of $\sim 2.5 \times 10^4 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. It is demonstrated that the obtained mobility values are highly reproducible.

As we show that surface adsorption has a large impact on field effect mobility, further studies should be directed towards minimizing the adsorbates and analysis of surface properties. An improved design of the measurement setup

allowing for heating and better evacuation of the sample space is likely to facilitate a further desorption of adsorbates. Exposing the devices to UV-light during evacuation, which may assist desorption, can also be investigated [31]. Further, passivating the nanowire surface by removing the native oxide followed by application of a high quality dielectric likely reduces surface adsorption. Possible methods are atomic hydrogen cleaning [47] or chemical etching followed by dielectric deposition [48]. Alternatively, by suspending the nanowires above a metallic gate using vacuum as a dielectric, one can minimize the effects of the substrate adsorption, leaving the wire adsorption as the predominant constituent affecting the field effect mobility. In the case of adsorbates creating a fluctuating potential profile along the wire resulting in charge scattering, a core-shell structure is expected to yield a higher field effect mobility because the potential fluctuations due to adsorbates are spatially separated from the channel owing to the shell. Finally, to study the surface composition of the nanowire and the substrate, x-ray photoelectron spectroscopy or Auger electron spectroscopy could be used [49].

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