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High yield of self-catalyzed GaAs nanowire arrays grown on silicon via gallium droplet positioning

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Abstract

We report and detail a method to achieve growth of vertical self-catalyzed GaAs nanowires directly on Si(111) with a near-perfect vertical yield, using electron-beam-defined arrays of holes in a dielectric layer and molecular beam epitaxy. In our conditions, GaAs nanowires are grown along a vapor–liquid–solid mechanism, using *in situ* self-forming Ga droplets. The focus of this paper is to understand the role of the substrate preparation and of the pre-growth conditioning. Without changing temperature or the V/III ratio, the yield of vertical nanowires is increased incrementally up to 95%. The possibility to achieve very dense arrays, with center-to-center inter-wire distances less than 100 nm, is demonstrated.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Defect-free III–V material integration on silicon is a goal, pursued for more than 40 years. The reason is that complete success would bring about future devices combining extremely interesting advantages of direct bandgaps, high carrier mobility and large solar spectrum coverage with the mature, cost-effective and high performance Si platform. Although great progress has already been made in terms of material quality for III–V layers grown on silicon, structural defects are still a challenge for critical device applications, such as lasers and high mobility transistors. These defects include misfit and threading dislocations, due to the large lattice mismatch between most III–V and silicon [1, 2], antiphase domain boundaries and cracks, due to polarity issues and thermal mismatch, respectively [3–5].

III–V nanowires benefit from a larger surface-to-volume ratio and are thus inherently able to relax strain more efficiently; this was shown theoretically [6, 7] and experimentally [8, 9]. Thanks to this unique property, the

first successful growth of vertical III–V nanowires on silicon were reported some years ago [10–13]. Recently, progress has been demonstrated in the controlled growth of gold-free III–V nanowires [14–18]. These are the most promising candidates for electronics, optoelectronics or energy applications because they permit compatibility with silicon technology by avoiding the introduction of detrimental midgap defects [19].

Despite the high level of control already demonstrated by a few groups over gold-free III–V nanowire shape, dimension and position on silicon [20–22], few studies have addressed in detail the processing and growth mechanisms making this control possible. The most successful nanowire arrays are reported to proceed via a particle-free, selective-area mechanism described in [21] for metal–organic vapor phase epitaxy (MOVPE). A complex preparation procedure was employed to achieve this yield (InAs/Si) and was described in [20]. It was proposed recently that group-III-assisted nanowire growth could also be possible under similar growth conditions, despite the absence of particles after growth [23]. There are at present very few reports on group-III-particle-assisted nanowire arrays and none on GaAs nanowires grown with a high vertical yield [22, 24].

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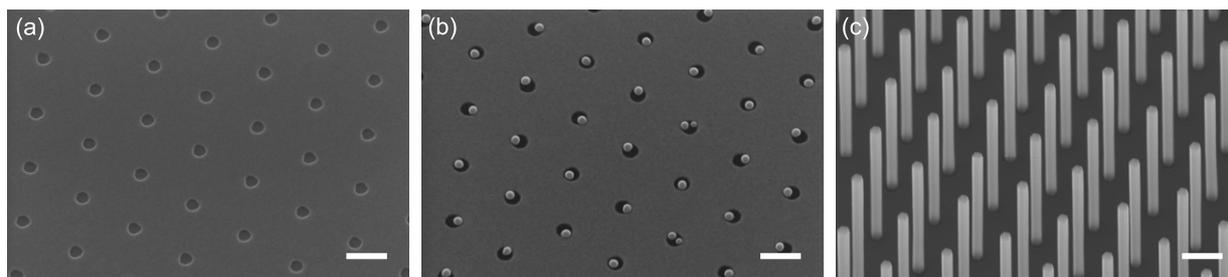


Figure 1. 30° tilted SEM images of the different steps used in this study: (a) hole array defined into the dielectric layer on an Si(111) substrate using electron beam lithography and etching, (b) gallium droplets formed *in situ* before nanowire growth, with controlled diameter to fit into the holes and (c) GaAs nanowire array growth assisted by Ga droplets in a vapor–liquid–solid growth mechanism. The scale bar corresponds to 200 nm.

The scope of the present study is to give insights into the key parameters leading to a high yield of self-catalyzed, vertical nanowire arrays on silicon. Ga-assisted GaAs nanowires grown by MBE have been chosen as a model system for this study. First, processing steps are discussed and their influence on the growth quality is analyzed. Then, the preparation of the samples and the droplet formation are discussed along with the growth mechanism to incrementally achieve a yield of vertical nanowires close to perfection.

2. Experiments

Figure 1 illustrates the three main steps followed to study the growth of vertical nanowire arrays, from the patterning of the dielectric layer (figure 1(a)) to the *in situ* droplet formation (figure 1(b)) and nanowire growth (figure 1(c)). Each of these steps is described in a separate section below.

2.1. Pre-growth processing steps

The aim of the pre-growth processing step is to allow a precise positioning of the nanowires on a silicon substrate. Silicon dioxide (SiO₂) grown by thermal oxidation and silicon nitride (SiN) deposited by plasma-enhanced chemical vapor deposition (PECVD), have been used as a mask to define the hole arrays on a (111) P-doped silicon substrate. The growth of SiO₂ and the deposition of SiN were adapted to obtain thicknesses ranging from 5 to 31 nm, as measured by ellipsometry. A polymethyl methacrylate (PMMA) resist was subsequently spin-coated and baked at 180 °C for 30 min in an oven, resulting in a thickness of about 100 nm. Electron beam lithography was performed using a VISTEC EBPG 5000+ beam writer at high energy (100 keV) and reduced beam current (100 pA), giving a spot size estimated at 5 nm. After a dose optimization step, several hole arrays have been defined with diameters ranging from 20 to 200 nm and inter-hole center spacing (itches) ranging from 60 nm to 1 μm. This allows us to investigate the effects of the hole size and the hole density on the nanowire growth in a single run. The patterns were transferred by reactive ion etching (RIE) using a PlasmaLab 80 chamber from Oxford Instruments, with a 13.56 MHz driven parallel plate reactor. Optimized chamber conditions were used to promote anisotropic etching using

a CF₄/CHF₃/Ar mixture and an SF₆/Ar mixture applied to SiO₂ and SiN etching, respectively. Since up to a week could separate a hole array processing batch and the actual nanowire growth, a quick chemical etching is needed, prior to the introduction of the samples into the ultra-vacuum environment, to remove the SiO₂ native oxide in the holes. Consequently, after resist stripping, samples have been dipped in a 1% hydrogen fluoride acid (HF) solution for 1 min prior to loading into the MBE chamber. Finally, after a thermal degassing at 200 °C for 1 h under ultrahigh vacuum conditions, samples were loaded into the MBE chamber and the temperature was ramped directly to the growth temperature, always much lower than the temperature required to thermally deoxidize silicon (~800–900 °C).

2.2. Nanowire growth procedure

Growth runs are performed in a Riber 32 P gas source molecular beam epitaxy (GS-MBE) reactor, using a high temperature cracked AsH₃ source (As₂ molecular flow) and a standard effusion cell for gallium. Growth rate and V/III ratios are calibrated using reflection high energy electron diffraction (RHEED) specular intensity oscillations. It was shown previously that the V/III ratio and temperature are the key parameters controlling nanowire diameter, length and morphology [22, 25, 26]. In the following, these growth parameters are kept exactly constant for all samples; temperature is set at 630 °C, As/Ga growth rate equivalent ratio is 1.8 and 2D equivalent GaAs growth rate is set at one monolayer per second. Under these conditions the nanowires have a diameter of 60 nm (±5 nm) and a length of 1 μm (±50 nm) on native-oxide-covered silicon substrates, used as a reference sample for the study of nanowire arrays. The aim of using this standard growth recipe is to deconvolute the influences of growth and pre-growth parameters (sample technological processing, chemical etching and pre-growth preparation) for the realization of high quality nanowire arrays. When the growth temperature is reached and stable, a Ga pre-deposition step is introduced for some of the growth, as mentioned in the following. This Ga preparation of the surface is performed by opening the Ga shutter, without any As₂ flux, for a duration between 0 and 120 s. Morphology of droplets and nanowires is studied using a Zeiss Supra scanning electron microscope (SEM) operated at 15 kV.

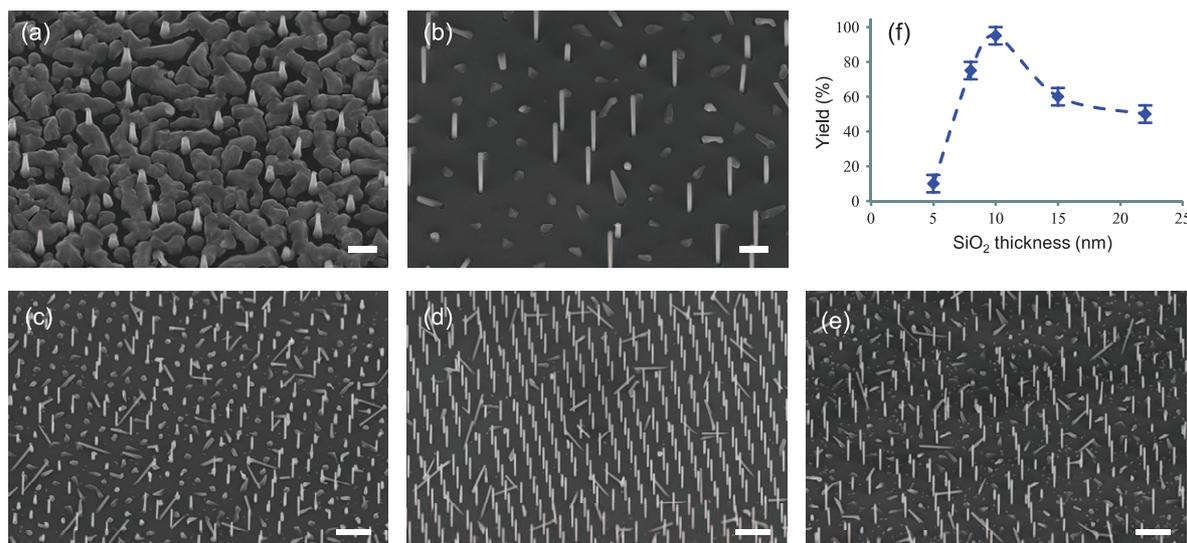


Figure 2. 30° tilted SEM images of the nanowire arrays. For all images, the hole diameter is 60 nm and the pitch of the array is 500 nm. The scale bar corresponds to 400 nm in (a) and (b) and to 1 μ m in (c)–(e). (a) 20 nm thick SiN layer with parasitic bulk growth, (b) 20 nm thick SiO₂ layer without parasitic bulk growth, (c)–(e) nanowire arrays for respectively a 5, 15 and 25 nm thick SiO₂ layer and (f) evolution of the yield as a function of the SiO₂ layer thickness.

3. Results and discussion

3.1. Influence of the dielectric layer

The influence of the dielectric layer on nanowire growth yield was first evaluated. In the literature, SiN and SiO₂ are both used to pattern the Si(111) and the GaAs(111) surfaces for growth of nanowire arrays [15, 22, 27]. To compare these two dielectric layers, 20 nm of silicon dioxide was grown by thermal oxidation and the same thickness of silicon nitride was deposited by PECVD on two different samples (thicknesses given after the HF dip). Hole arrays are then formed as described in section 2 above, and GaAs nanowires are finally grown without any Ga pre-deposition. Figures 2(a) and (b) show 30° tilted SEM images of the resulting nanowire growth for SiN-based arrays and SiO₂-based arrays, respectively. In the first case (with an SiN layer), significant parasitic growth occurs (crystallites, rough polycrystalline layer) between nanowires, whereas in the second case (with the SiO₂ layer), the amount of parasitic growth is drastically reduced. Nanowire diameters are similar in both cases, but the length is smaller in the case of the silicon nitride pattern. The same phenomenon was also observed for 10 and 30 nm thick layers of both dielectric materials. This different behavior could be linked to a different chemical interaction between the gallium droplets and the dielectric layer [15]. Additional PECVD-deposited SiO₂ dielectric layers were also investigated. Parasitic growth was observed, as in the case of deposited SiN (not shown). It is suggested that growth selectivity differences on the dielectric masks are due to the preparation methods, which could lead to changes in surface chemistry and diffusion (lower quality of the deposited layers). Indeed, high quality GaAs nanowire arrays have been reported by others on (111)B GaAs substrates using an SiN dielectric layer and MOVPE [28]. Therefore, even if both dielectric

layers could in principle be used for nanowire positioning in MBE, the thermally grown silicon dioxide layer has been selected in our case and will be the only one used in the following.

After selection of the dielectric layer material, the influence of its thickness on nanowire growth was studied. Because of the HF dip just before the loading into the MBE chamber, the thickness of the SiO₂ layer is overall reduced from 10, 21 and 31 nm to respectively 5, 15 and 25 nm. Standard growth parameters were used for these samples without gallium pre-deposition. Figures 2(c)–(e) present the nanowire arrays obtained for each of these thicknesses. In all cases, the parasitic growth is completely avoided. We also noticed that lengths and diameters of nanowires grown in patterns are similar to the ones of nanowires grown on a control sample piece (same epitaxy run), which shows that hole arrays are not affecting the nanowire growth significantly. By defining ‘standard nanowires’ as 1 μ m long vertical nanowires (± 50 nm) with diameters of 60 nm (± 5 nm), a yield for each array can be calculated. This yield is illustrated in figure 2(f) as a function of the SiO₂ layer thickness. An optimum is extracted for 60 nm diameter nanowires around 10 nm. This optimal dielectric layer thickness is not significantly affected by the pitch of the array.

3.2. Influence of Ga pre-deposition

Since the nanowires studied in this work are grown via a vapor–liquid–solid (VLS) mechanism [22], the gallium droplet formation is a key parameter governing the nucleation. Even without intentional gallium pre-deposition, droplets can spontaneously form, due to the very low V/III ratio used for growth. After growth, the droplet will be present or not on the top of the nanowire, depending on the cooling-down conditions [22, 23]. The influence of surface pre-conditioning

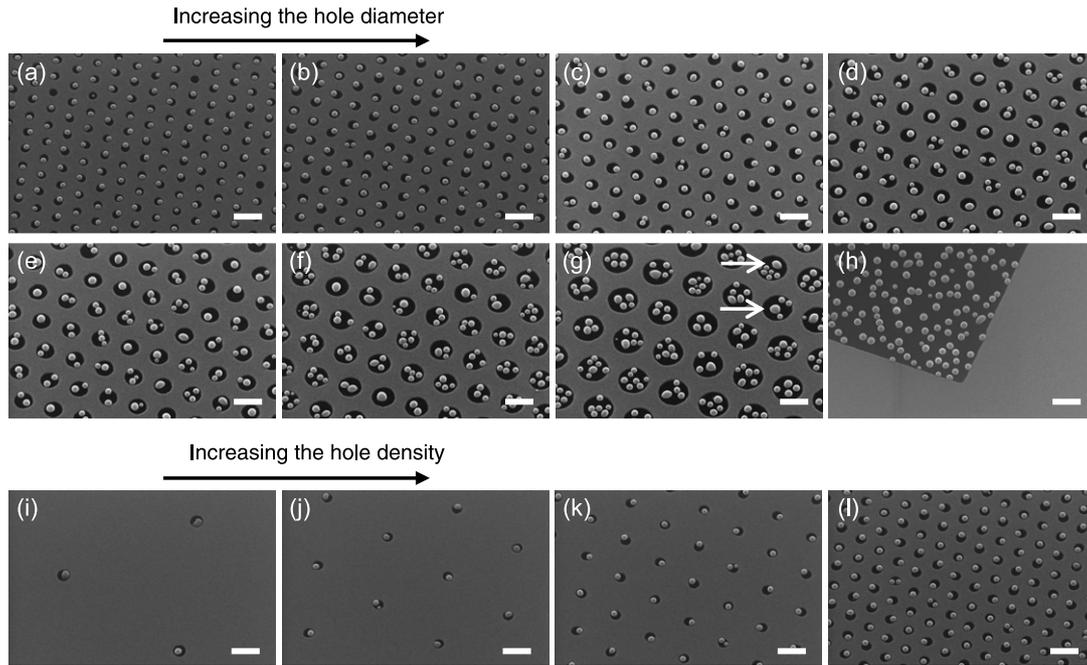


Figure 3. 30° tilted SEM images of gallium droplets created in the arrays. The scale bar corresponds to 200 nm in all figures. (a)–(h) Evolution of the number and the diameter of the droplets as a function of the hole diameters: respectively 40, 60, 80, 100, 120, 150 and 200 nm (for respectively 140, 160, 180, 200, 220, 250 and 300 nm pitches) and a large opening. (i)–(l) Evolution of the droplets as a function of the pitch of the hole arrays (respectively 1 μm , 500, 250 and 100 nm between each hole). The diameter of the holes is 60 nm.

with Ga droplets was studied by evaporating gallium on a sample (20 nm thick SiO_2 mask) at 1 ML s^{-1} (growth rate measured for a GaAs 2D layer) during 45 s. This sample was cooled down under vacuum conditions and analyzed by SEM.

Figure 3 shows the gallium droplets created in the hole arrays (20 nm thick SiO_2) for increasing hole diameters between 40 and 200 nm (a)–(g) and for decreasing pitch between 1 μm and 100 nm (i)–(l). First, no gallium droplet can be found on the SiO_2 layer, which proves that Ga droplets can only form or be maintained in oxide-free openings. For the layer thickness illustrated in this figure, the 20 nm diameter holes were probably not completely opened during processing, resulting in the absence of Ga droplets (not shown). For 40 nm holes (figure 3(a)), there is a one-to-one correspondence between holes and droplets. The droplet size increases with the hole diameter from 35 to 50 nm (figures 3(a)–(d)) when a single droplet forms. The first ‘double’ droplets appear for diameters around 60 nm (figure 3(b)) but they have a smaller diameter (around 25 nm). It is suggested that two droplets could nucleate at different positions within a hole and are in competition to collect the gallium adatoms. Finally the number of droplets in the holes increases with the hole diameters (figures 3(c)–(g)); their close proximity sometimes leads to merging small droplets into a bigger one (see arrows in figure 3(g)). Figure 3(h) shows the case of an infinitely large hole (100 μm opening in the mask layer); in this case, the droplet diameter is similar (~ 50 nm), but with lower dispersion (no small droplet) and the density is slightly lower. This suggests that the droplet diameter is mostly controlled by the growth conditions (Ga duration and temperature).

Figures 3(i)–(l) show the effect of the hole density on the droplet creation. The amount of gallium evaporated is the same for all samples and the hole diameter is 60 nm. It is worth noting that the droplet diameter is not affected by the hole density over the investigated range. To get more insight into this observation, one can roughly evaluate the quantity of gallium adatoms present in the droplet and compare it to the quantity of gallium nominally evaporated in the holes. Equation (1) gives the amount of gallium adatoms in a droplet (approximated as a perfect sphere) and equation (2) gives the amount of gallium evaporated in a hole:

$$n_d = \frac{\rho N_a V_d}{M} \quad (1)$$

where n_d is the amount of gallium adatoms in the droplet (with the assumption of negligible re-evaporation), ρ is the volume mass of the gallium in a liquid droplet (g cm^{-3}), N_a is Avogadro’s number, M is the atomic mass of the gallium (g mol^{-1}) and V_d is the droplet volume (cm^3):

$$n_h = \Gamma T_d D_{\text{Ga}} S \quad (2)$$

where n_h is the amount of gallium adatoms evaporated in the hole, Γ is the growth rate (ML s^{-1}), T_d is the duration of the deposition step (s), D_{Ga} is the density of adsorption sites (sites/ML cm^2) [29] and S is the hole surface (cm^2).

To find out the origin of the gallium adatoms present in the droplets, direct evaporation or surface diffusion, n_d and n_h , were calculated for the observed 35 nm droplets in 60 nm holes and we obtained n_d around 1.2×10^6 and n_h around 0.8×10^6 . Therefore, the number of atoms found in a droplet

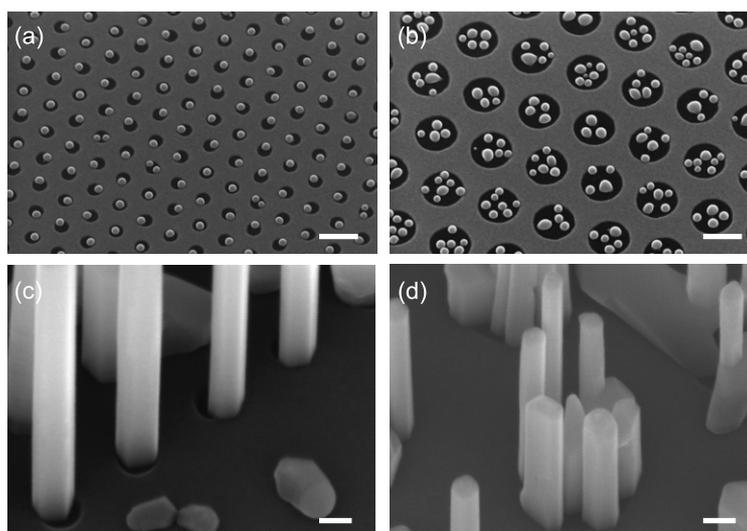


Figure 4. 30° tilted SEM images of gallium droplets and GaAs nanowires. The scale bar corresponds to 200 nm in (a) and (b) and to 50 nm in (c) and (d). (a) Gallium droplets in 60 nm holes (b), gallium droplets in 200 nm holes. (c) GaAs nanowires grown with the droplets presented in (a) and (d) GaAs nanowires grown with the droplets presented in (b).

is very close to the number of atoms evaporated in a hole. This could be interpreted by two different scenarios. The first one is that gallium re-evaporates quickly on both the Si and the SiO₂ surfaces (in and out of the holes). In that case, the gallium adatom diffusion length should be long enough to compensate for evaporation, and the gallium present in the droplets should originate from a large collection area. This in turn implies a competition between the droplets with increasing areal density, which is not observed (see figures 3(h) and (i)–(l)). The second scenario is that the gallium evaporation rate is fast on the SiO₂ surface but remains low on the Si surface (in the holes). As n_d and n_h are comparable, gallium present in the droplet should mainly originate from what is evaporated in the holes or in close proximity (<20 nm). In this scenario, the hole density should not influence the droplet size until very small pitches, because gallium evaporated on the SiO₂ will be re-evaporated before it can diffuse into the holes. Despite the simplicity of this approach, this second scenario is in good agreement with the evolution illustrated in figures 3(i)–(l). Hence these observations are explained by Ga re-evaporation coefficient differences between Si and SiO₂.

3.3. Direct link between droplets and nanowires

Once the droplets are formed on the sample, both arsenic and gallium fluxes are opened to nucleate and grow the nanowires. Figure 4 presents the evolution of the patterns before and after the growth of the nanowires for two hole diameters. Figures 4(a) and (c) correspond to the 60 nm holes whereas they are 200 nm in figures 4(b) and (d). In the first case nanowires nucleate preferentially on the side of the holes, which is in agreement with the positioning of the droplets and was also observed by others [27]. It is also possible to observe that the nanowire diameter is slightly smaller than the hole as presented in our recent work [22]. For the 200 nm pattern, multiple droplets lead to the growth of multiple nanowires in a

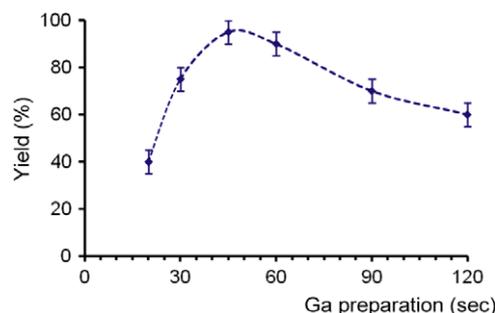


Figure 5. Evolution of the yield of 'standard' nanowires as a function of the gallium preparation time (in seconds). The gallium flow was set at 1 ML s⁻¹ for a 2D GaAs layer, the hole diameter is 60 nm, the SiO₂ thickness is 10 nm and the growth temperature is 630 °C.

single hole. Both the number and diameter of nanowires and droplets are in good agreement. This illustrates nicely the VLS mechanism governing growth, in our case. Figure 4(d) shows that nanowires separated by only a few nanometers (<10 nm) are able to grow without merging, which is very positive for the prospect of future ultra-dense nanowire arrays. However, at such a huge areal surface density, nanowire length can differ significantly. This could be explained by considering a sidewall diffusion-limited axial growth rate, which is inversely proportional to nanowire diameter.

3.4. Influence of the gallium preparation step on the yield

Figure 5 presents the yield of 'standard' nanowires grown in 60 nm holes, 500 nm pitch, as a function of the gallium amount evaporated prior to growth. There is an optimum around 45–60 s, which corresponds to droplets around 30–40 nm. For shorter durations the yield quickly decreases and islands are instead observed in the holes. For bigger droplets (longer durations), the yield slowly decreases for the 60 nm array

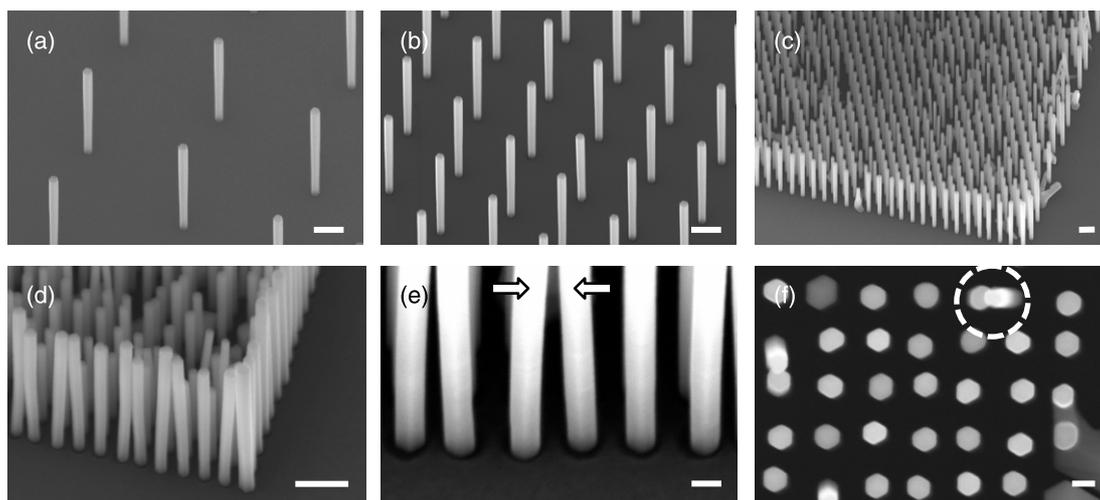


Figure 6. Nanowire arrays with different pitches. The scale bar corresponds to 200 nm in (a)–(d) and to 40 nm in (e) and (f). The hole diameter is 60 nm, the SiO₂ thickness is 10 nm, the growth temperature is 630 °C and the preparation time of gallium is 45 s. (a)–(b) 30° tilted SEM images of nanowire arrays with a yield over 95% and a pitch of respectively 1 μm and 500 nm, (c) yield over 85% for the 100 nm pitch, (d) yield over 75% for the 80 nm pitch, and (e)–(f) respectively 30° and 0° tilted SEM images of the 80 nm pitch array.

whereas it increases for the 80 nm pattern. In this case, the nanowires have a larger diameter (around 70 nm in diameter) and a shorter length.

The amount of gallium deposited prior to the growth changes the droplet diameter and could change its shape by affecting the contact angle between the droplet and the Si substrate. Consequently, obtaining perfect arrays of diameter-controlled nanowires requires some calibration of Ga pre-deposition duration, optimal dielectric layer thickness and growth parameters (temperature and V/III ratio).

3.5. Influence of the pitch of the pattern

Finally, the influence of the pitch of the array on nanowire growth was considered. Figure 6 shows the evolution of the nanowire array morphology with increasing density for 60 nm holes and 45 s of gallium evaporated prior to the growth. The pitches are respectively 1 μm in figure 6(a), 500 nm in figure 6(b), 100 nm in figure 6(c) and 80 nm in figure 6(d). Figure 6(e) shows a high magnification image of an array with a nanowire inter-center distance of 80 nm, close to the Si/GaAs interface (30° tilt angle), and figure 6(f) shows a top view high magnification image of the same array (0° tilt angle). Due to the charging effect during SEM inspection, neighboring nanowires can merge at such a high areal surface density (see arrows in figure 6(e) and circle in figure 6(f)). The yield of vertical nanowires is over 95% and stable for pitches down to 250 nm, it decreases to 85% when reaching 100 nm (figure 6(c)) and to 75% for 80 nm pitch (figure 6(d)). The ‘filling factor’ of the 80 nm pitch array is around 19% (square array, 80 nm pitch, diameter of nanowires around 50 nm and yield 75%).

These results compare favorably with recent works on III–V nanowires in terms of areal density and diameter. Hertenberger *et al* reported a high yield of selective-area InAs nanowires grown by MBE on Si(111) [27] and a similar yield

for a pitch down to 250 nm, but with minimal nanowire diameters above 100 nm. Persson *et al* reported dense gold-assisted InAs nanowires grown on InAs(111)B with a pitch down to 150 nm and particle diameters ranging from 50 to 65 nm [30]. As diameter can be independently increased *in situ* in the Ga-assisted growth mechanism, by switching from VLS to lateral growth, the filling factor of the extremely dense nanowire arrays reported here can be adjusted depending on the type of applications. Dense arrays of very small or very large diameters could be obtained on demand. This will be important for future photovoltaic and thermoelectric applications, directly integrated on silicon. Moreover, results should in principle be applicable to In-nucleated III–V nanowires too (InAs, InP, InSb), as group-III-nucleated nanowires were demonstrated for these materials [31–33]

4. Conclusions

In conclusion, we have investigated the different parameters influencing the yield of nanowires grown in a hole array. The nature of the dielectric layer, the diameter of the holes and the gallium deposition prior to the growth have been found to be the key parameters to achieve the growth of highly controlled nanowire arrays, and more important than the actual growth parameters (temperature and V/III ratio). The bulk growth is completely avoided by the SiO₂ layer and the density of wires does not affect the growth until a pitch of 100 nm. The method presented here is general and can be applied to improve the yield of gold-free VLS-grown nanowire arrays on silicon for other III–V materials. We believe that the control and understanding reported in this work represents a promise for future integration of III–V devices on silicon.

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