Development of Dependable Network-on-Chip Platform (3)

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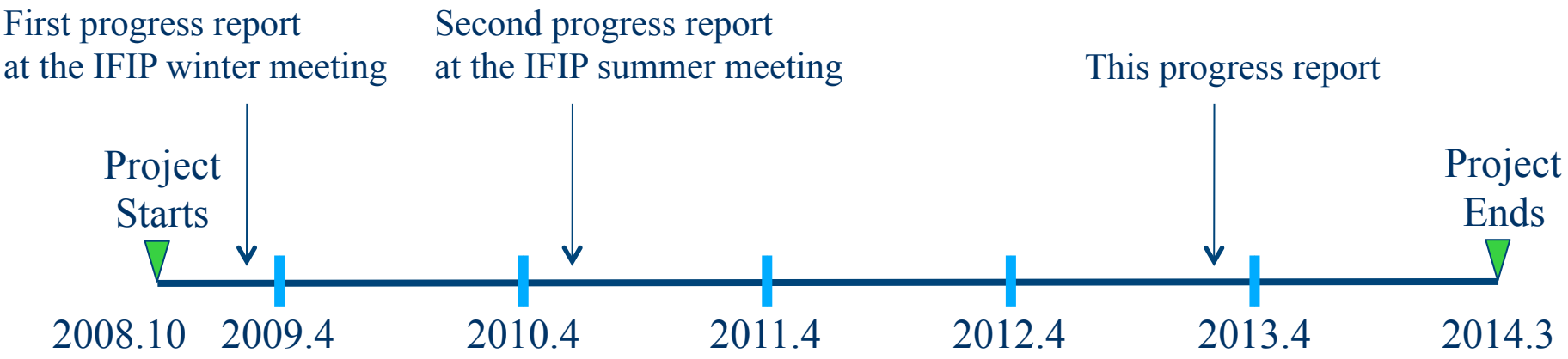
Project summary

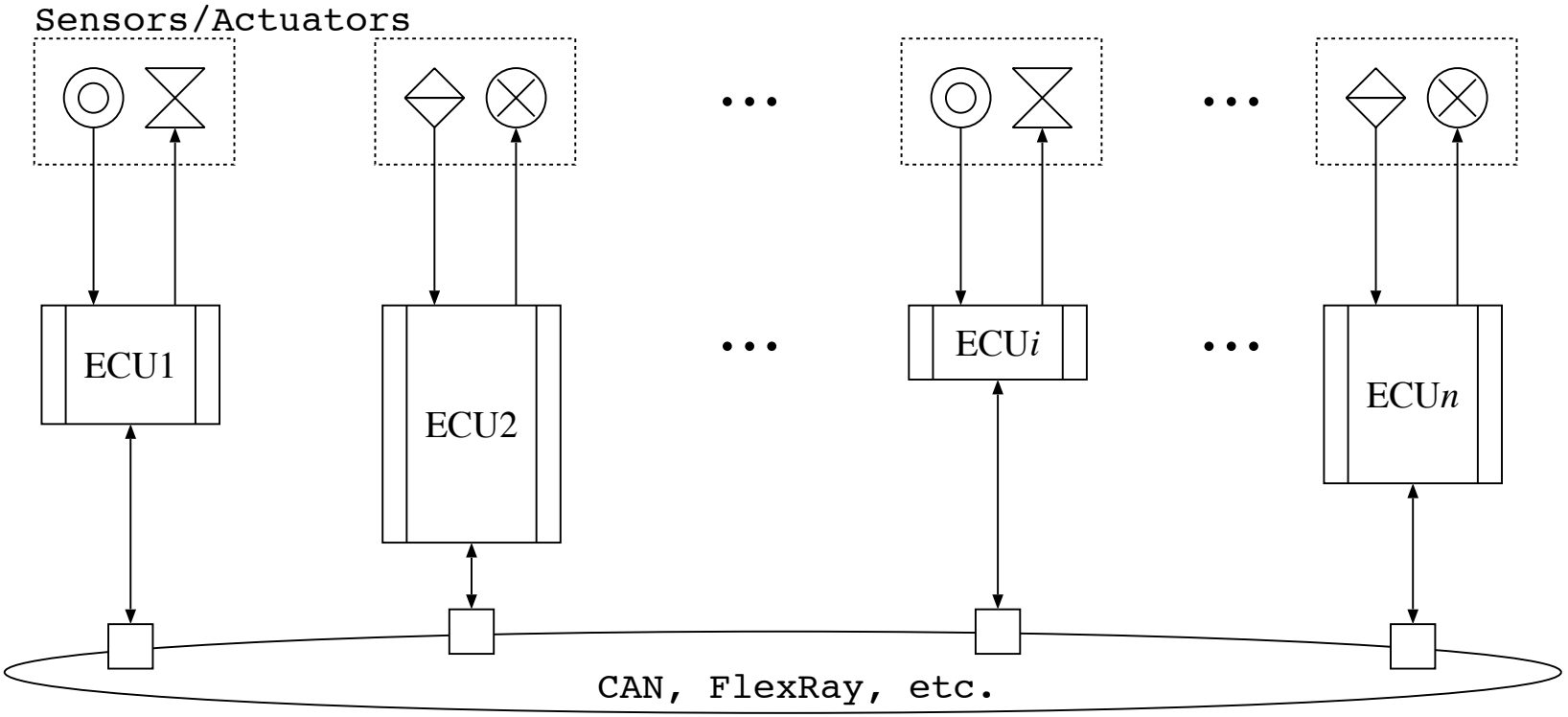
- 5.5 year National project (CREST)



- Goal
  - Platform for performing many and various tasks dependably, efficiently and adaptively
  - Demonstration in automotive control system area

Backgrounds

- Recent cars are equipped with many ECUs
  - Conventional ECU configuration



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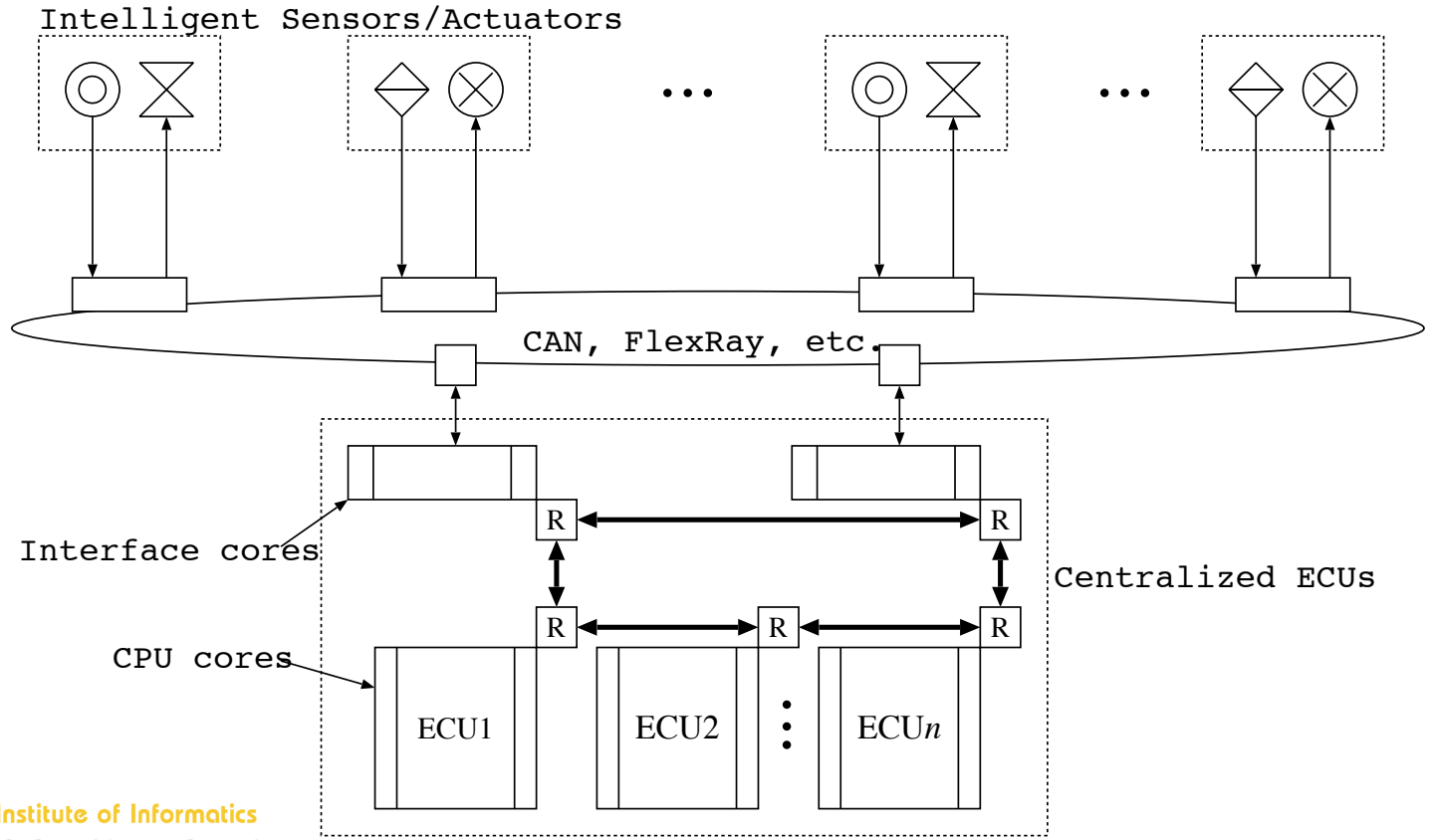
  - Centralized ECU approach



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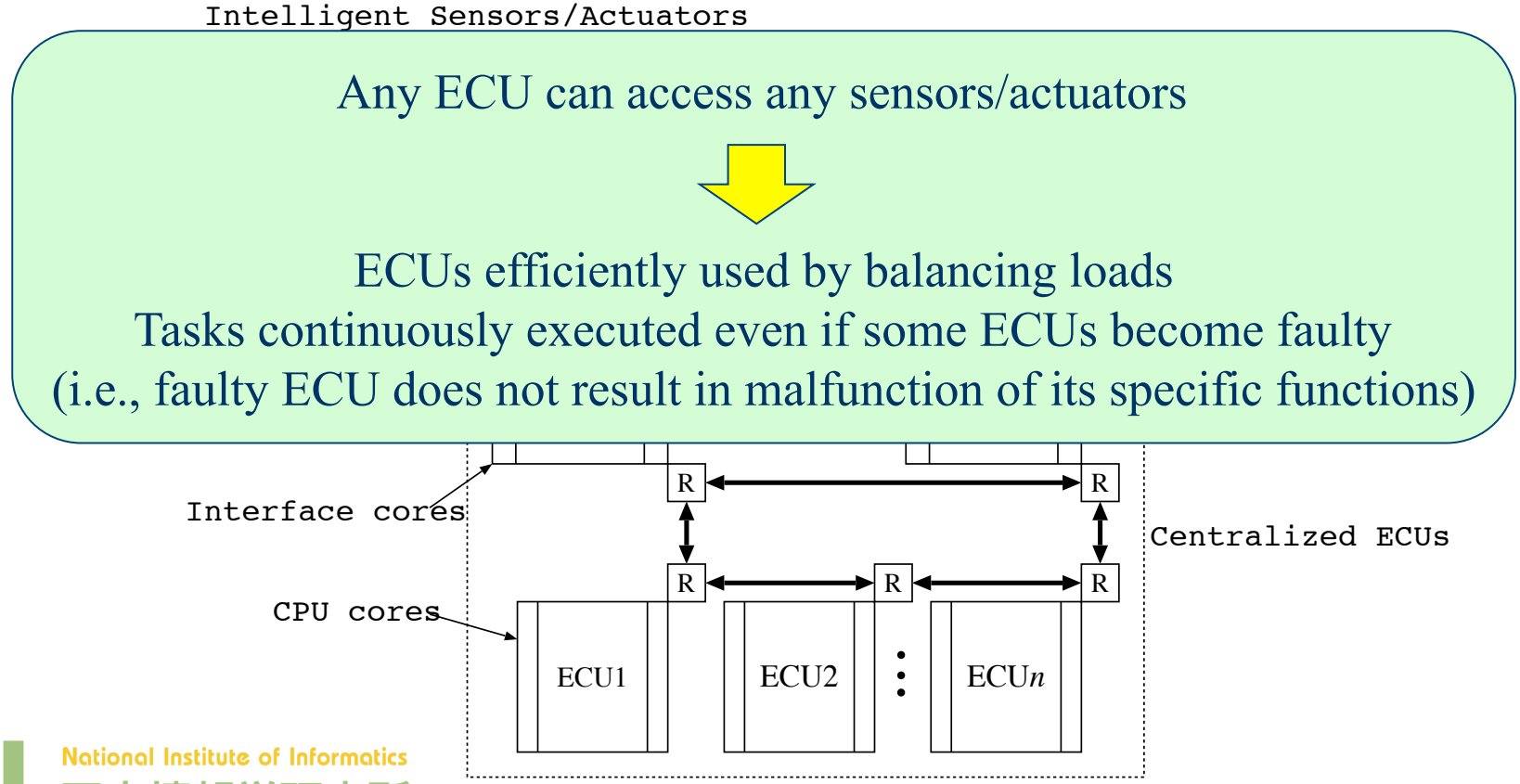

Backgrounds

- Centralized ECU approach
  - NoC (Network-on-Chip) based
    - Some European projects
      - Recomp: Reduced certification costs for trusted multi-core platforms. *http://atc.ugr.es/recomp/.*
      - Race: Robust and reliant automotive computing environment for future ecars. *http://projekt-race.de/.*
  - Multi-Chip NoC based [Yoneda, et al. PRDC2012]
    - Multiple NoCs are connected via off-chip links
      - On-chip networks seamlessly extended to multi-chip networks
    - Advantages
      - Cost-effective : small NoC chips are cheap, and various sizes of configuration are possible (without developing different sizes of NoCs)
      - Chip-level redundancy : tolerate a chip fault

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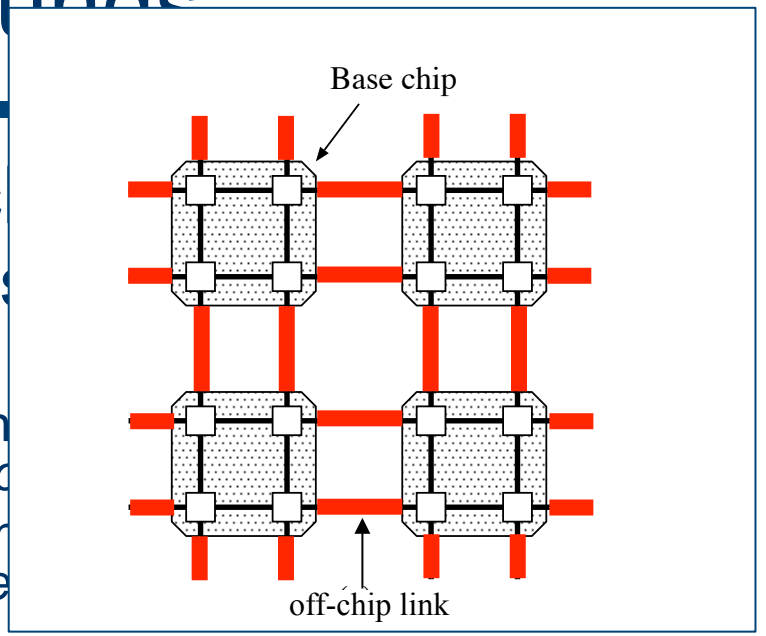
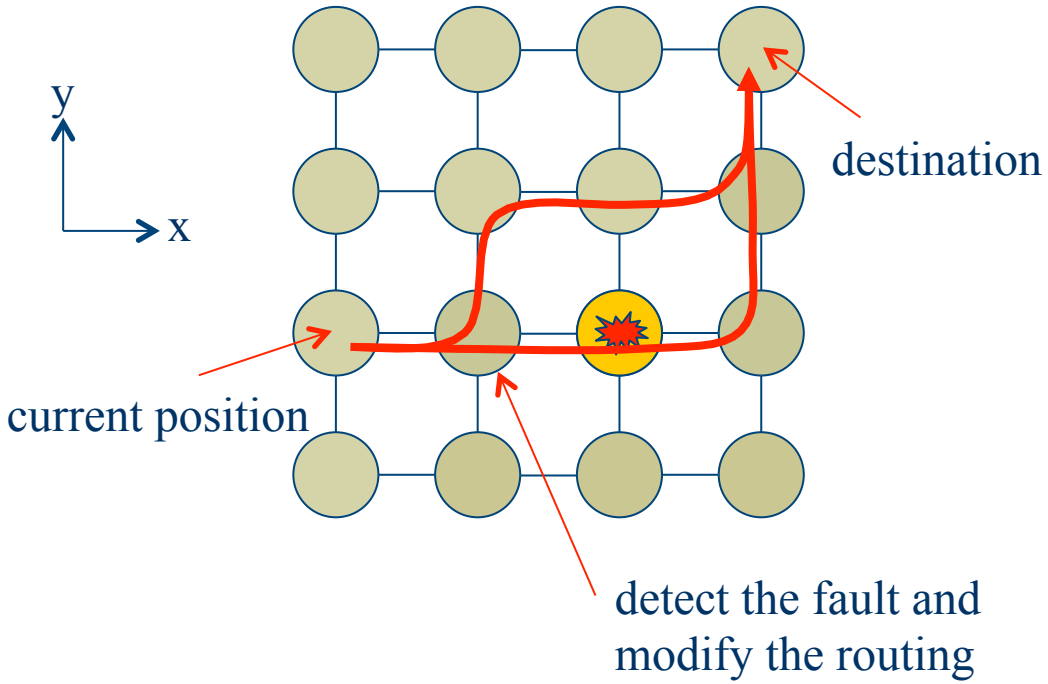


Outcome

- Hardware platform
  - Multi-Chip NoC
    - Fully asynchronous on-chip network
    - Dependable, adaptive, deadlock-free routing
    - Efficient inter-chip communication technology
- Dependable task execution
  - Pair & Swap
- Task allocation
  - Redundant allocation, redundant scheduling
- Demonstration of the proposed approach
  - Practical automotive application

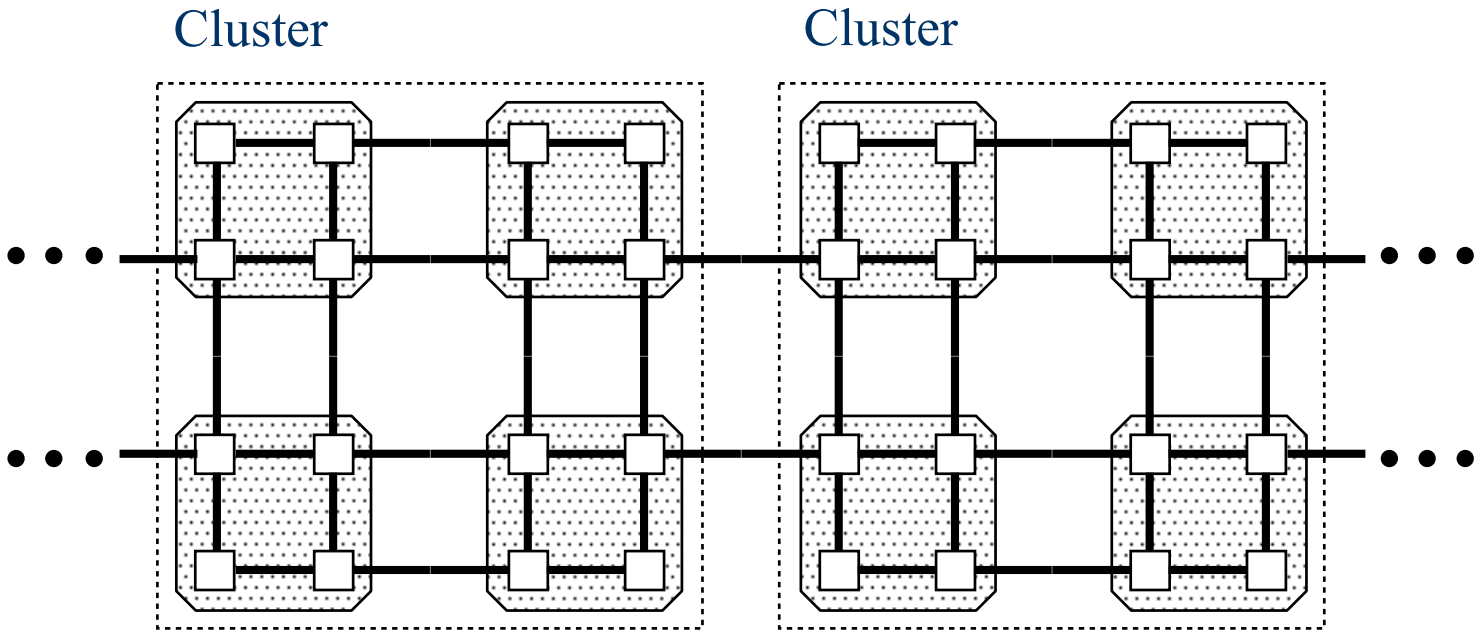
Fault tolerance in Routing level

- When a router goes faulty, a detour path will be taken



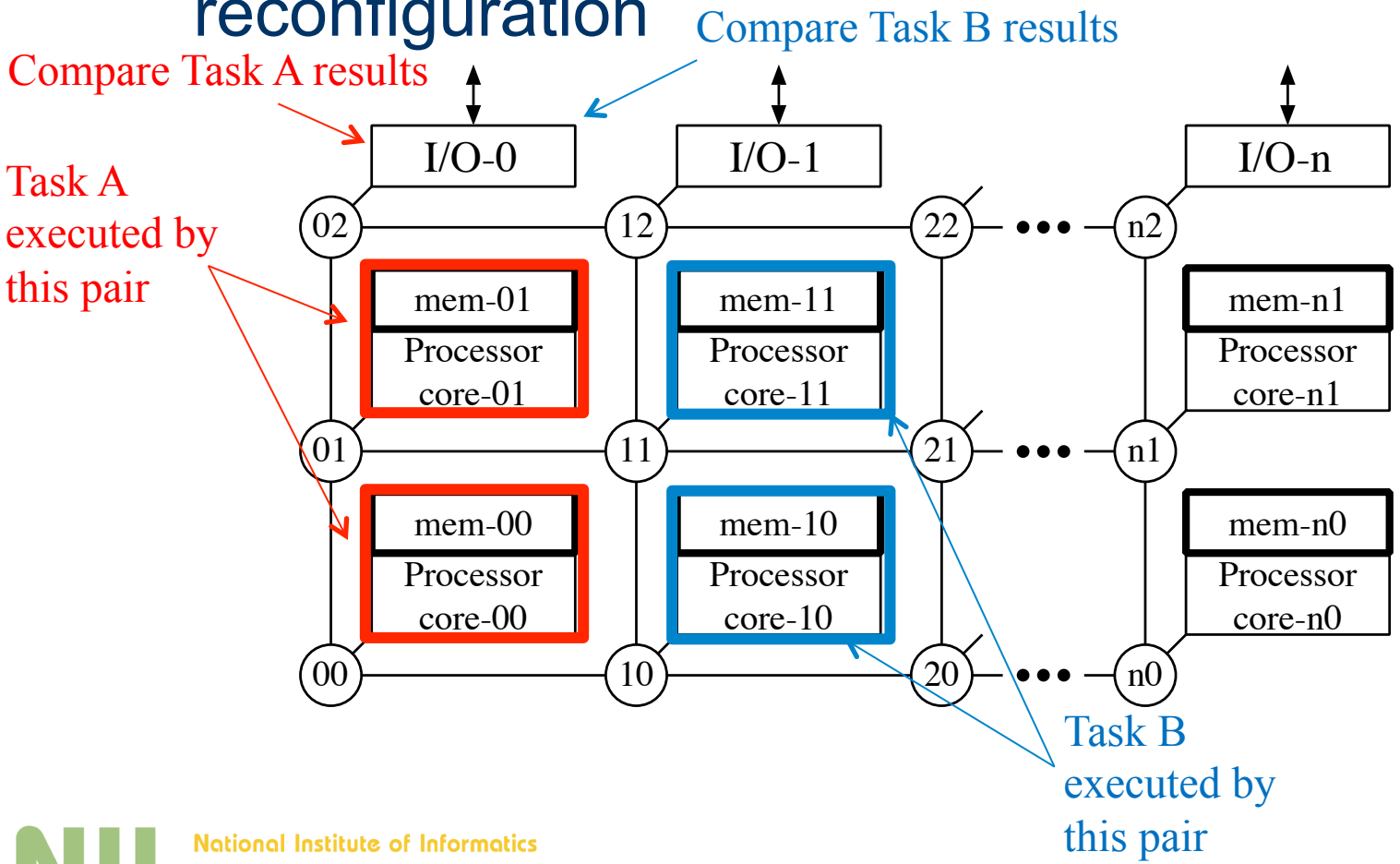
Fault tolerance in Routing level

- Single chip/router/link fault can be tolerated in each cluster



Dependability in Processor level

- Duplicated execution, comparison, and pair-reconfiguration



Pair & Swap

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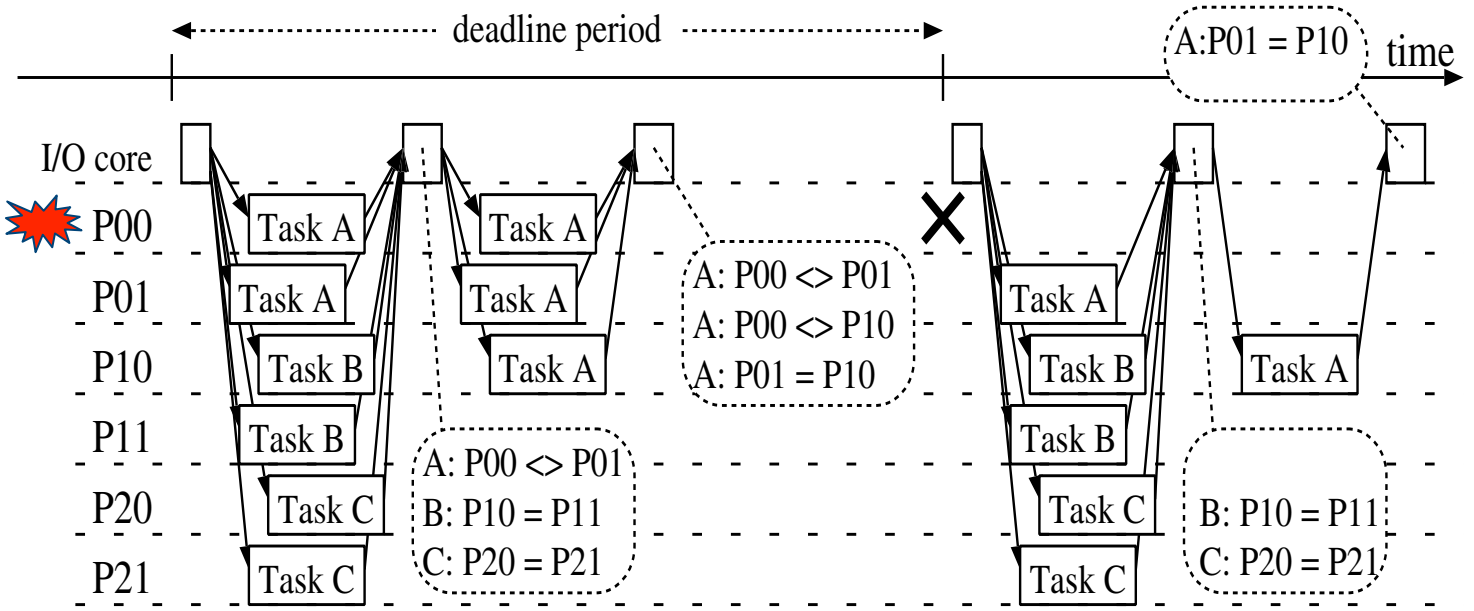
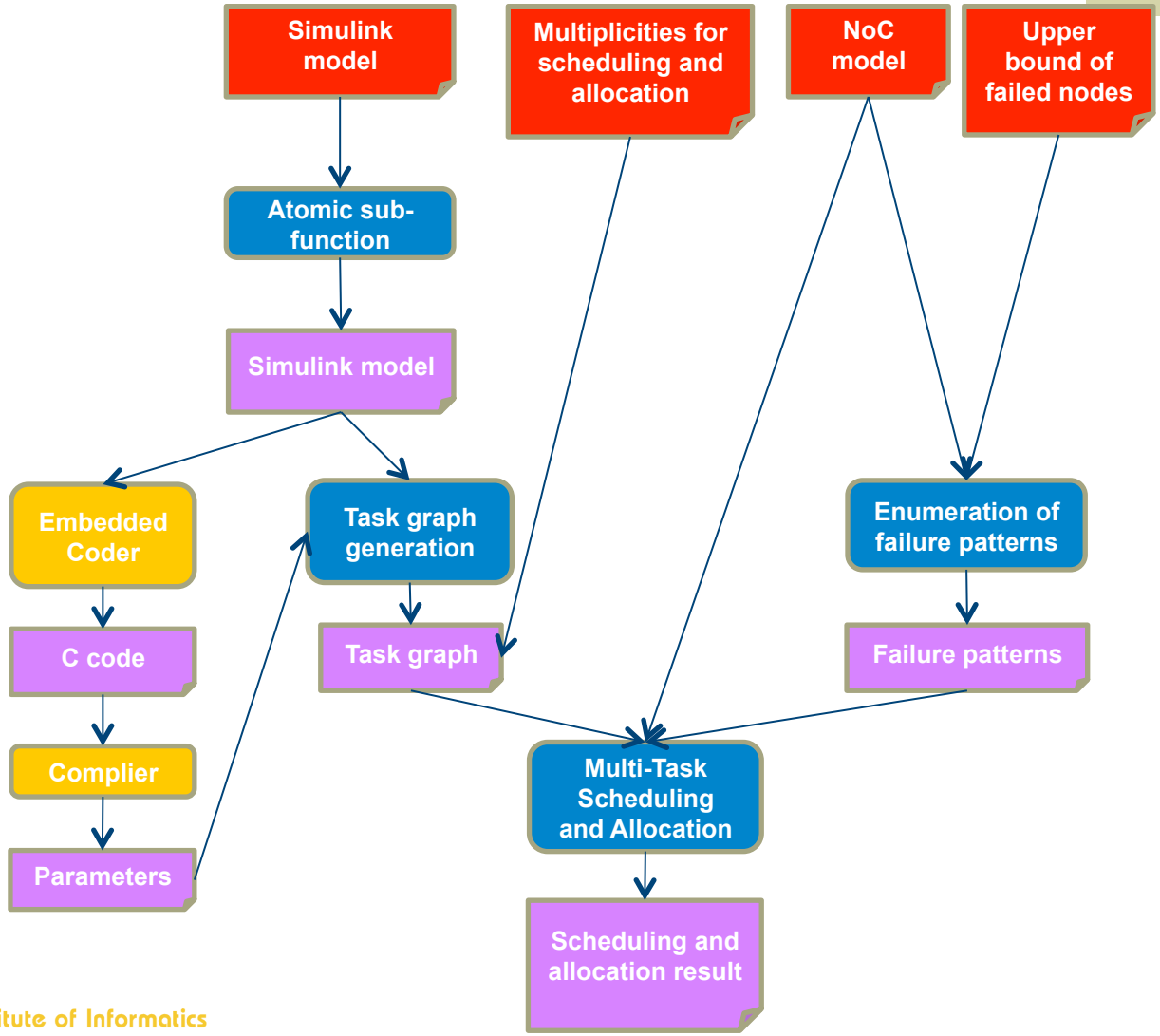
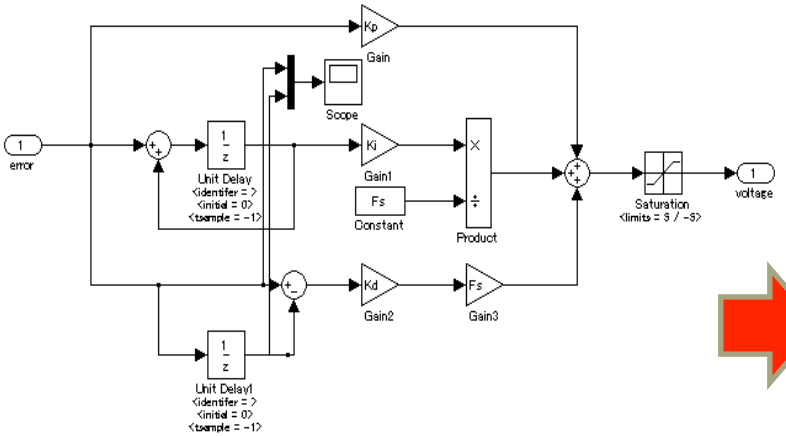


Tasks are redundantly loaded in several cores

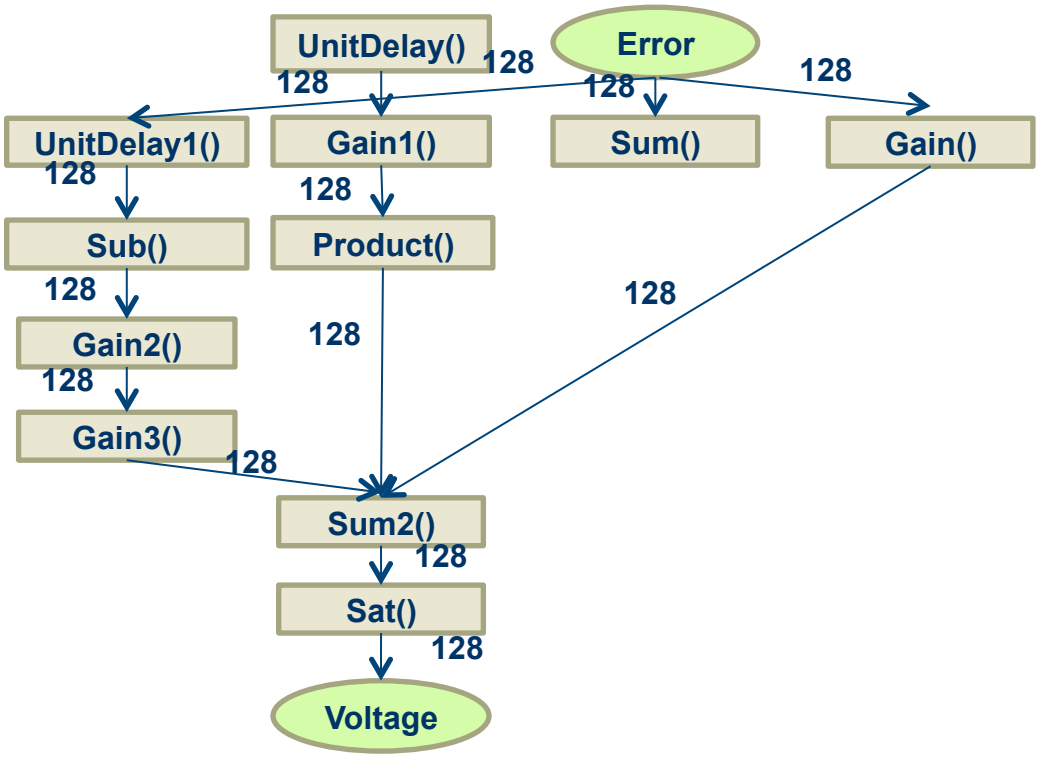
Task allocation



Task allocation



Task graph



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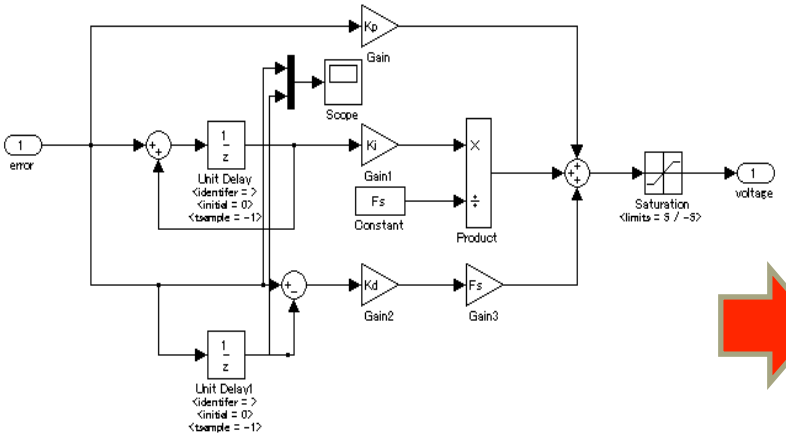

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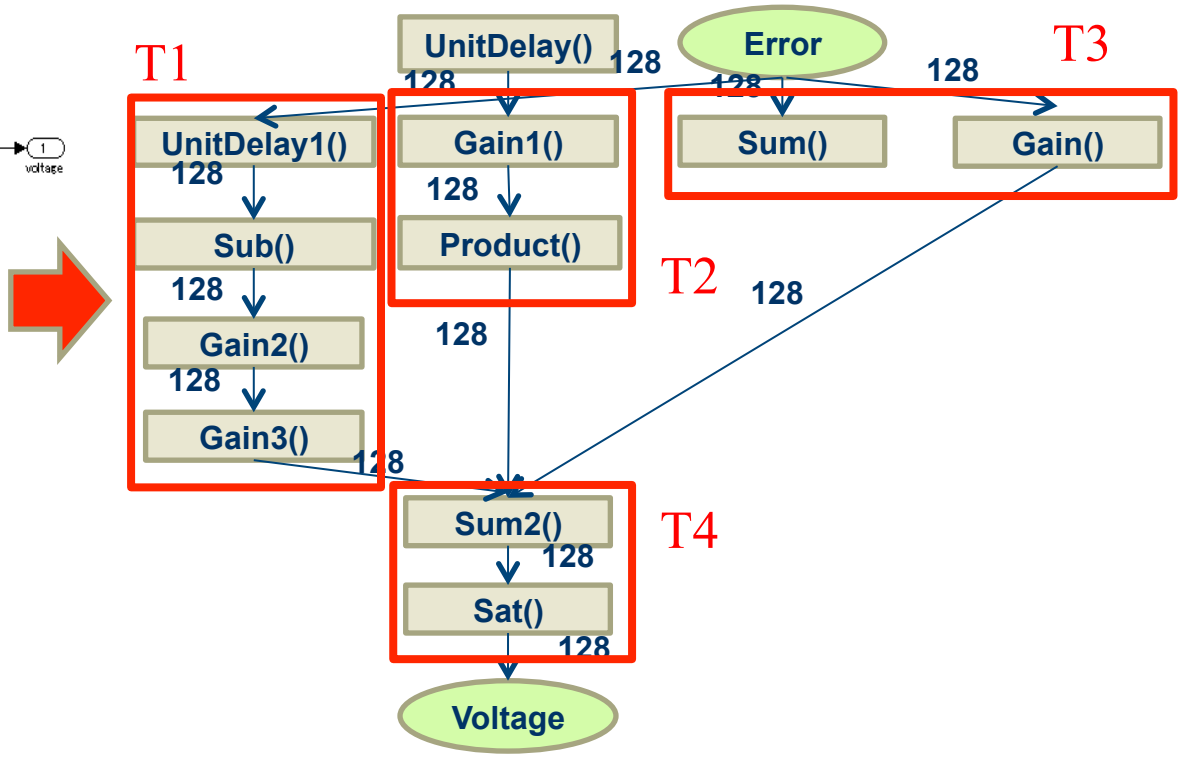
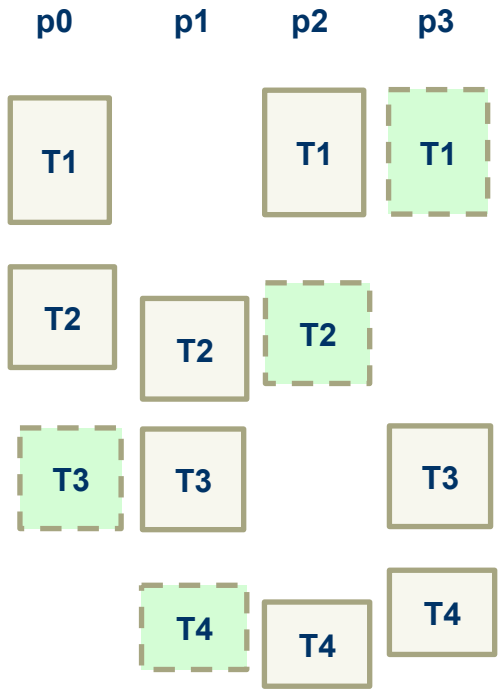


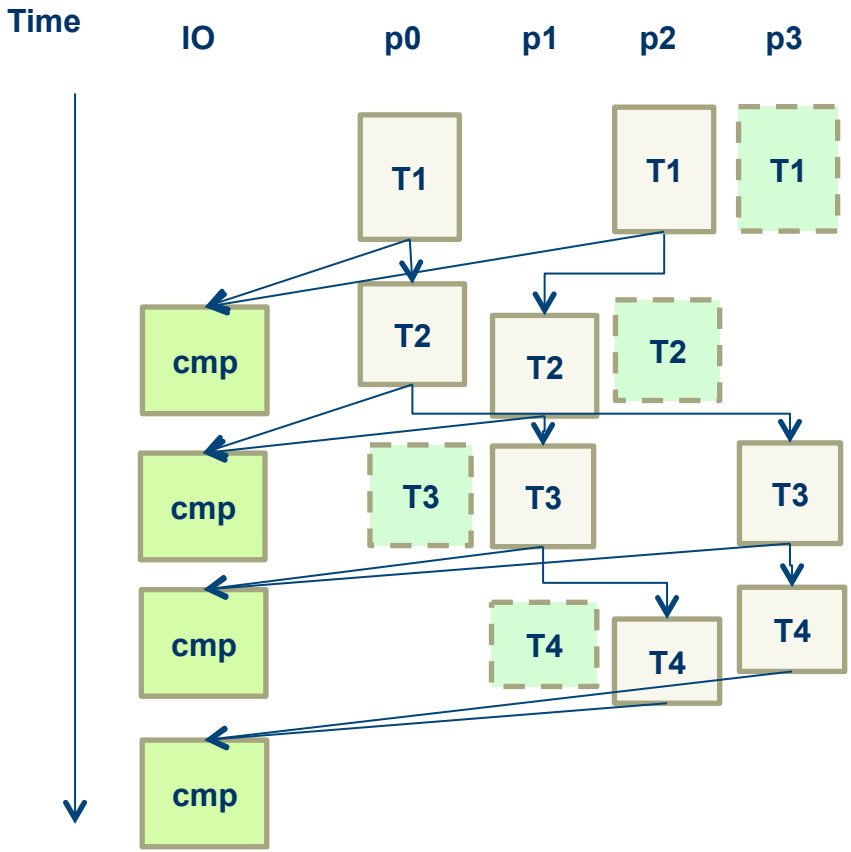
Task allocation

Tasks are allocated to CPU cores redundantly



Task scheduling

Duplicated execution and comparison



Demonstration

- Automotive Application
  - Integrated attitude control system for a four-wheel drive car
    - Torque, brake, and steering control of 4 wheels performed by ECUs
  - Highly cooperative process needed by each ECU
    - Integrated Control ECU
    - 2 Electric Power Steering Control ECUs
    - Brake Control ECU
    - Battery Management ECU

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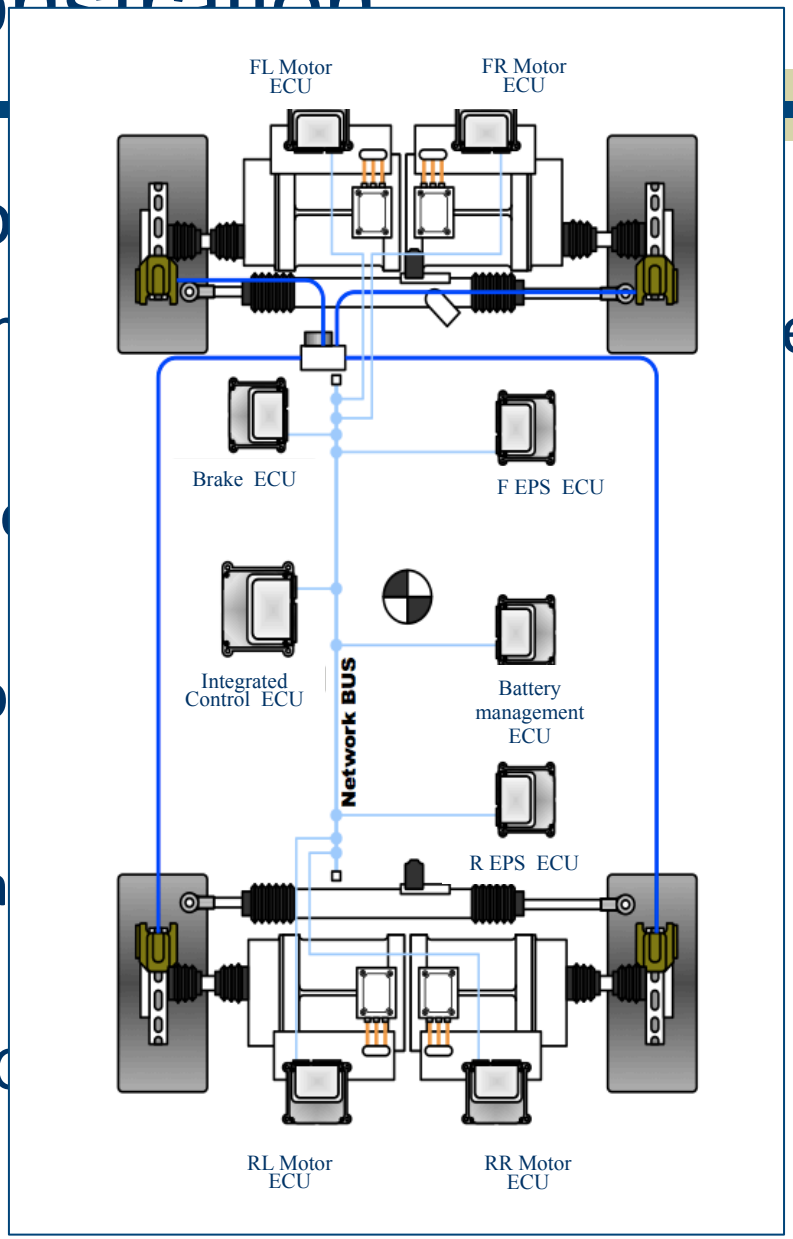
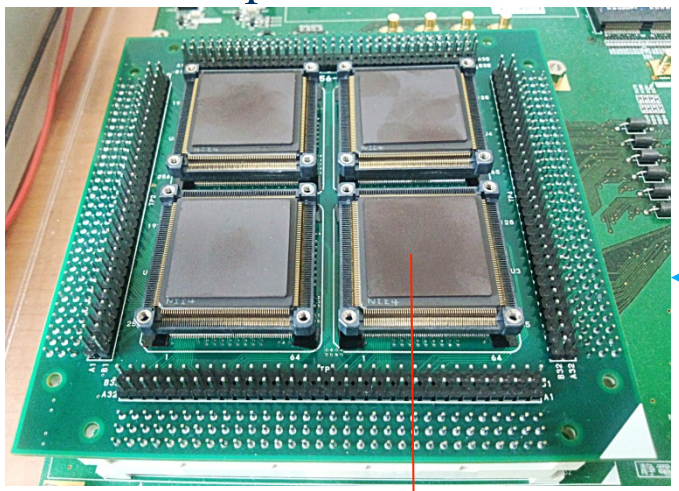


Demonstration

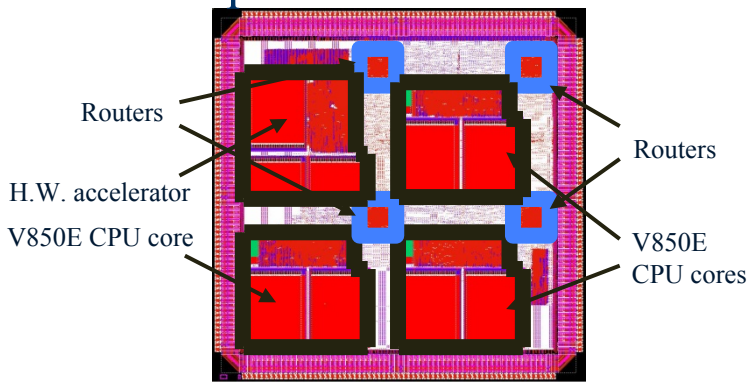
- Characteristics of this application
  - Stopping control is very dangerous
    - Higher availability is required

Experimental system

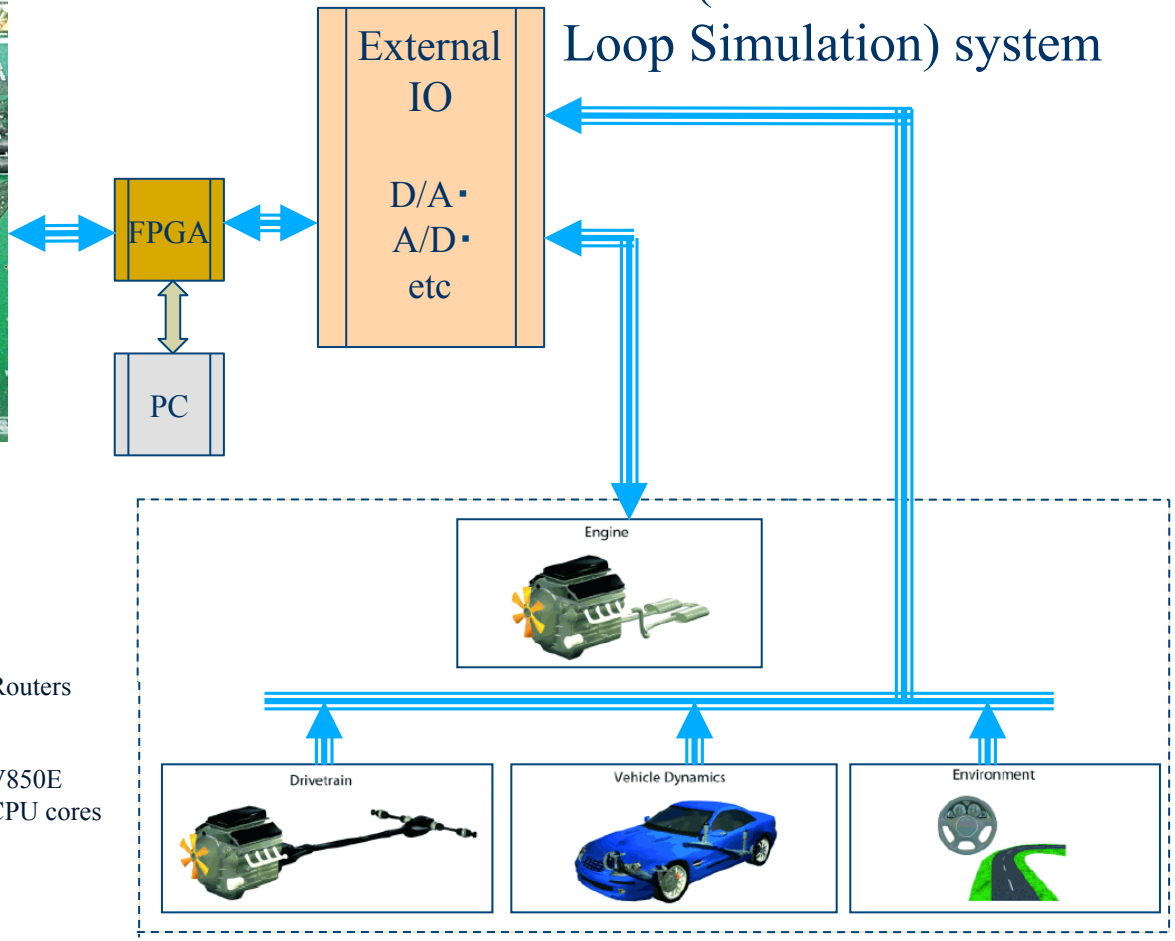
Base chip × 4



Base chip



HILS (Hardware In the Loop Simulation) system



Ongoing work

- Evaluation kit
  - Evaluation board
    - Dependable NoC platforms
      - 4 Multi-Chip ASICs
      - Vertex7(XC7VLX690T)
    - HILS interface
  - Pseudo HIL-plant models (executable on PC)
  - Redundant task allocation tool
    - Input: (Simplex) Simulink model for application
    - Output: Executable codes for redundant cores

Summary

- Provide a platform such that
  - Required dependability can be obtained by simply
    - connecting base-chips, and
    - allocating tasks redundantly
  - User just needs to prepare a simplex version of an application program