HITACHI
Inspire the Next

Fault Pathologies caused by Moore's Law, and Remedies

2011/07/03

Nobuyasu Kanekawa
Hitachi Research Laboratory,
Hitachi, Ltd.

HRL Hitachi Research Laboratory

HITACHI
Inspire the Next

Contents

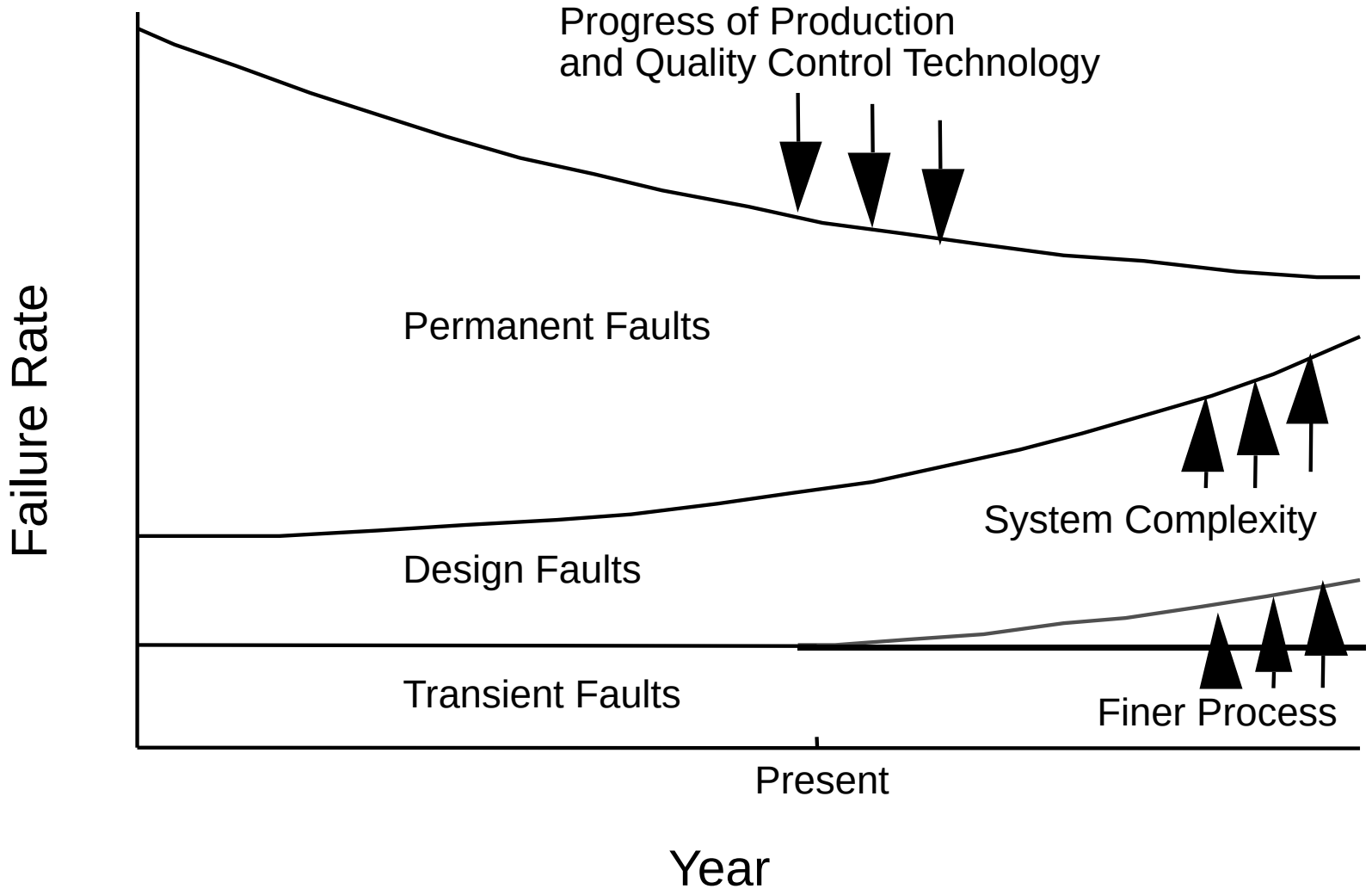
HRL Hitachi Research Laboratory

HITACHI
Inspire the Next

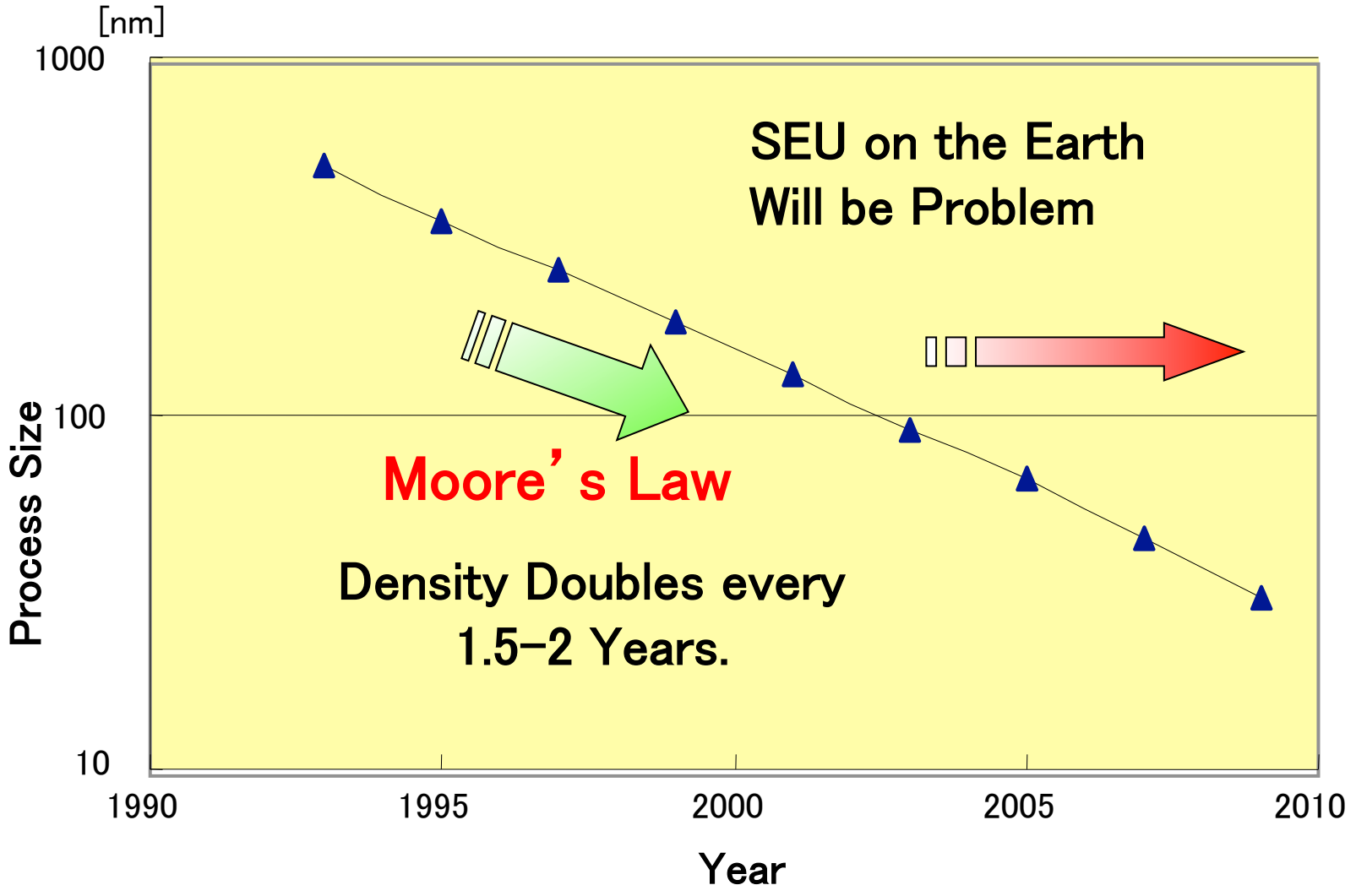
Contents

HRL Hitachi Research Laboratory

Trends in Failure Cause



Moore's Law



Terrestrial Neutron induced SEU's

HITACHI
Inspire the Next

Integration of Semiconductor Causes

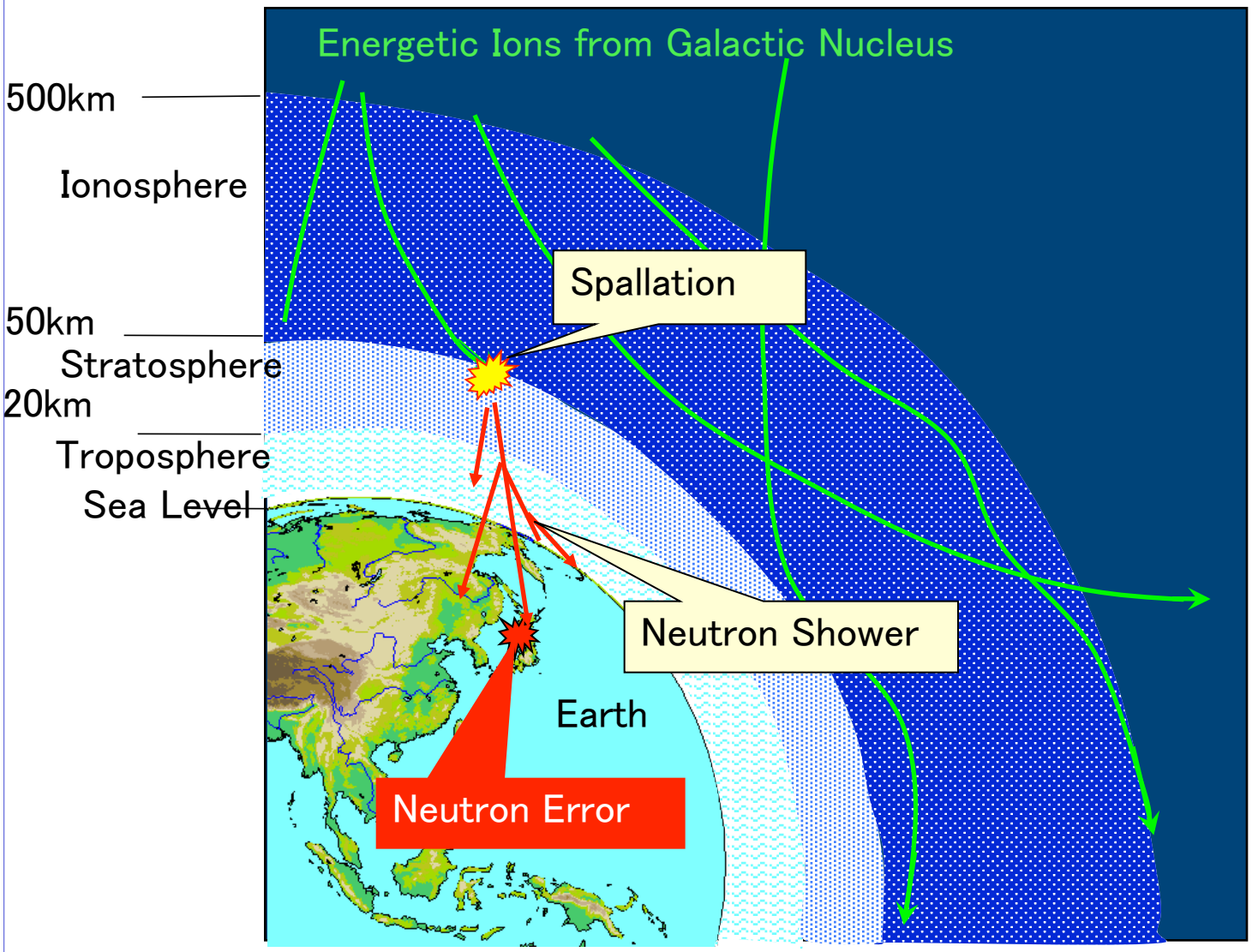
→ Decrease Funnel Area (Reduce Error Rate)

Decrease Critical Charge (Increase Error Rate)

→ Increase Error Rate in Overall

- Error Rate: x 1.5–2.0/Generation
- Memory Volume x *n*→# of Upset x *n*

Cosmic Neutron Induced SEU Mechanism



Synchronization Problem

HITACHI
Inspire the Next

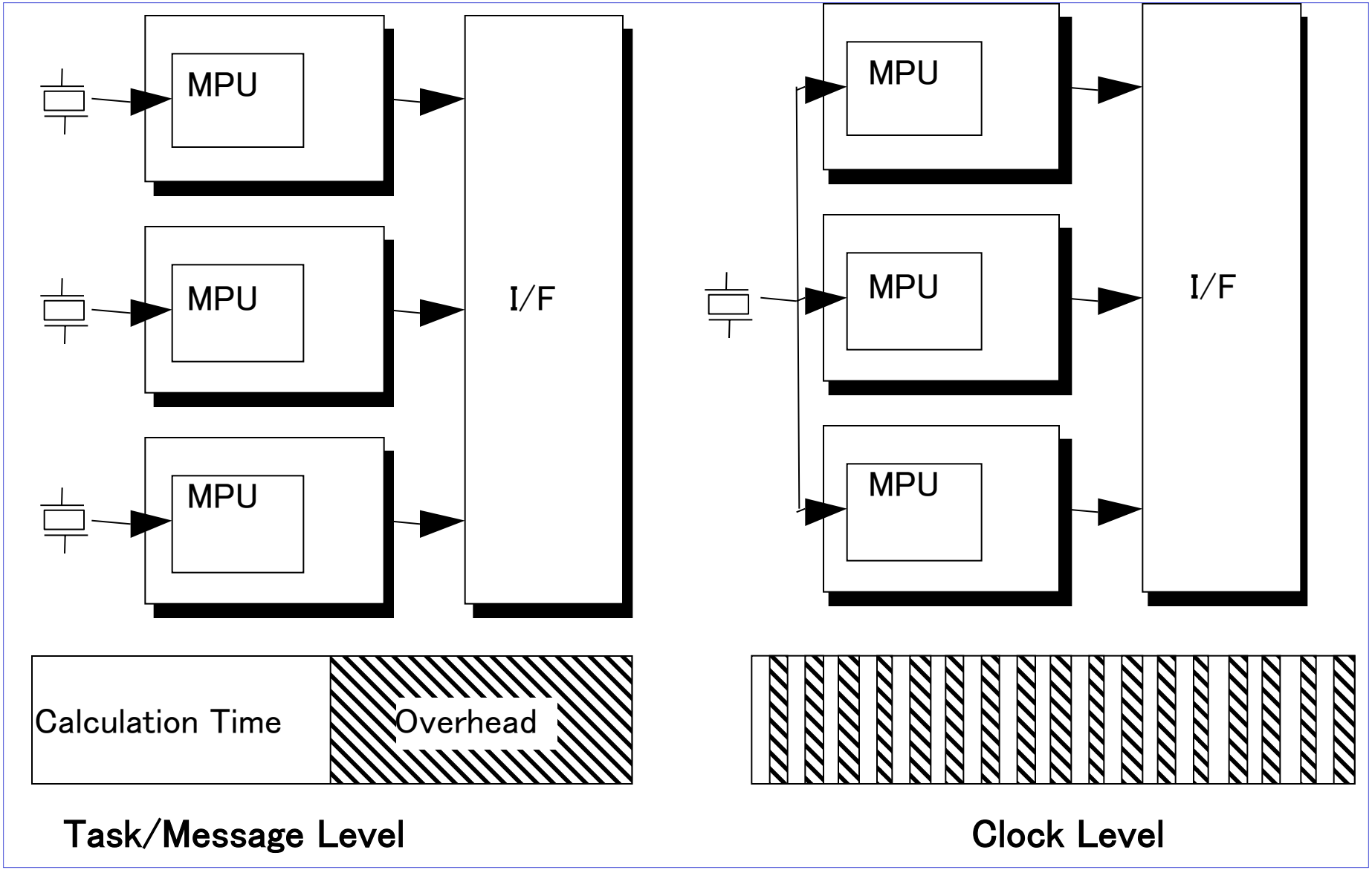
Integration of Semiconductor Causes

Higher Clock Frequency

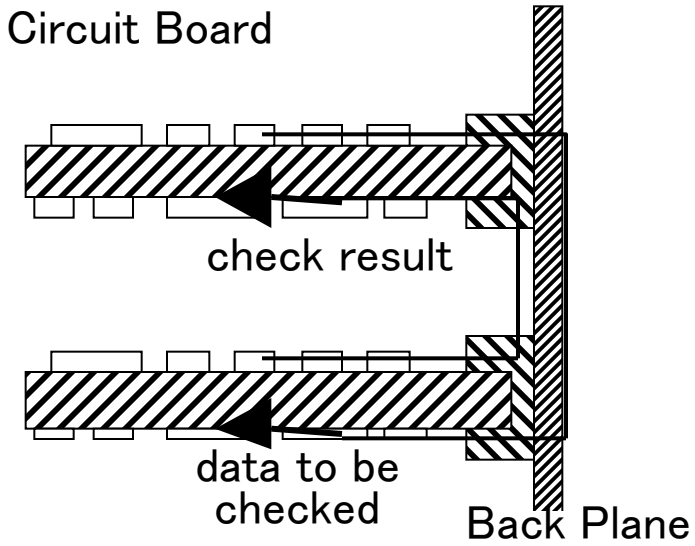
Consideration for Synchronization among Redundant Subsystems will be Indispensable

- Propagation Delay among Redundant Subsystems
  vs.
- Maintenance-ability (Replace-ability) of Redundant Subsystems

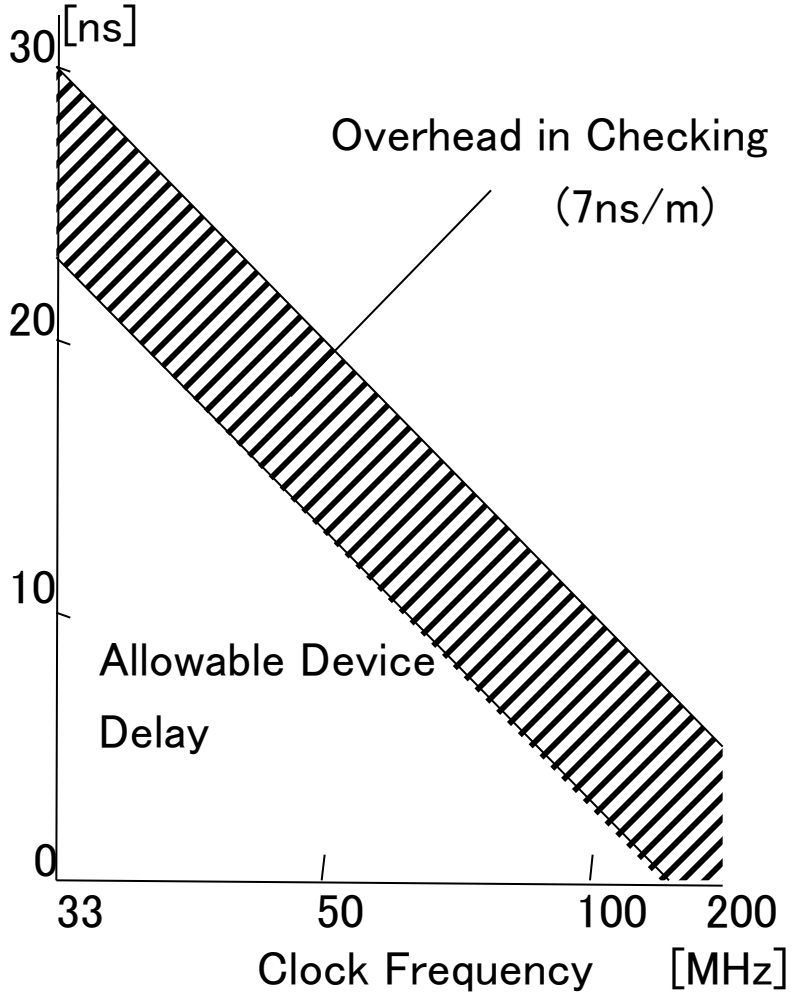
Synchronization and Overhead



Synchronization and Overhead



Signal Propagation Delay



Delay vs. Frequency

Electro-Magnetic Disturbance Sensitivity

HITACHI
Inspire the Next

Integration of Semiconductor Causes

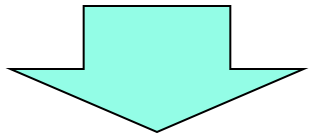
Higher Clock Frequency
Lower Power Supply Voltage
→Larger Noise Intensity
→More Noise Sensitive

Consideration for Electro-Magnetic Disturbances (EMC, Power Integrity) will be Indispensable

Pathologies and Remedies

HITACHI
Inspire the Next

- Terrestrial Neutron induced SEU's
- Synchronization Problem



Intra-Board Redundancy
On-chip Redundancy

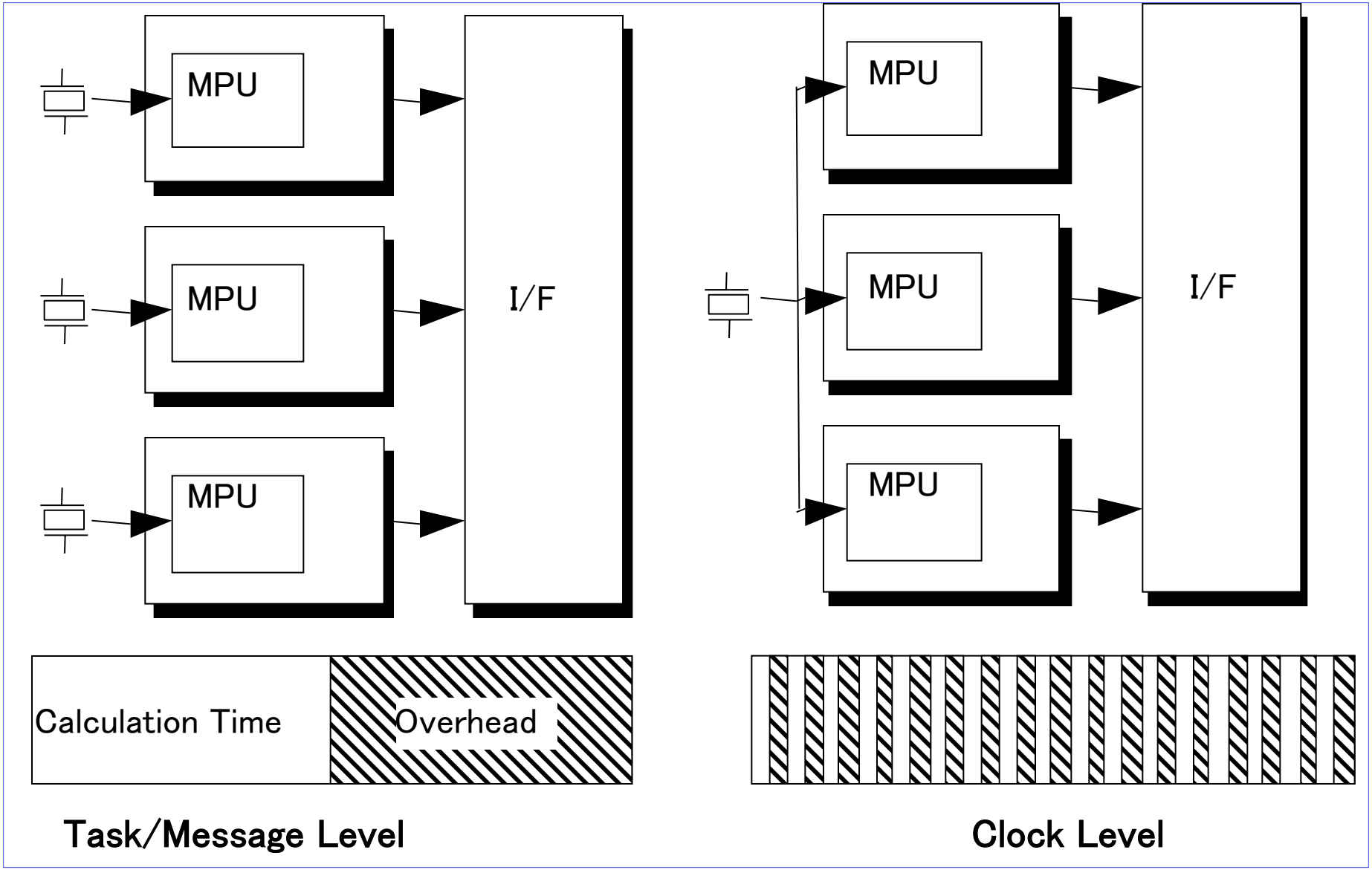
HITACHI
Inspire the Next

Contents

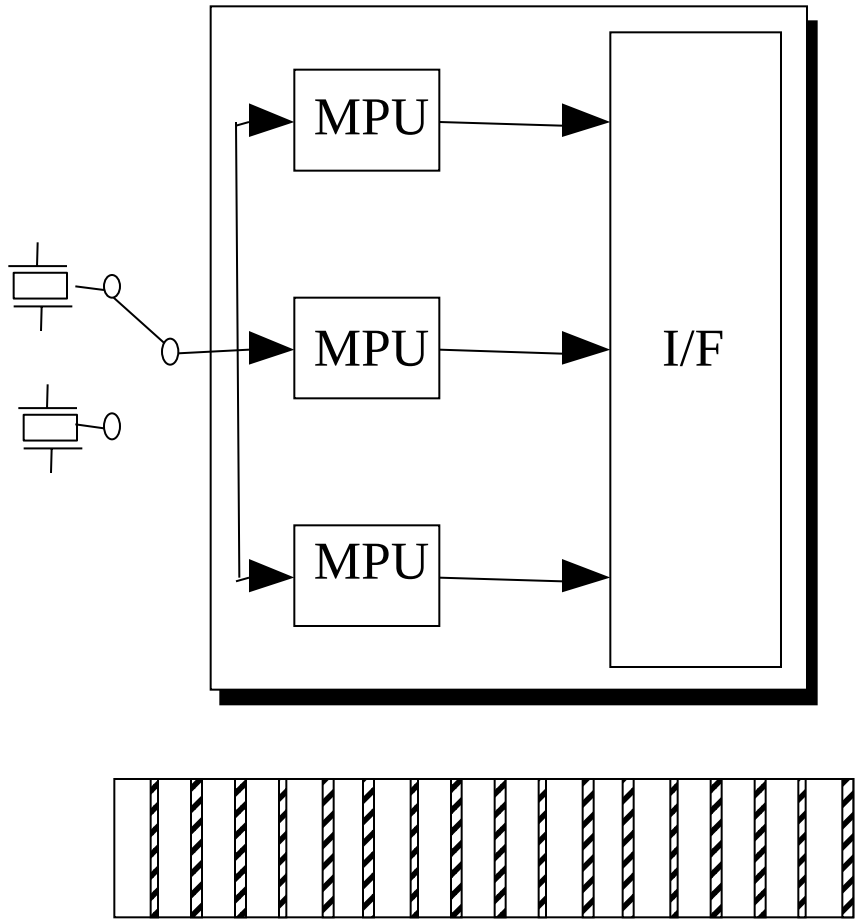
1. Fault Pathologies caused by Moore's Law
2. **Intra-Board Redundancy**
3. On-chip Redundancy
4. Conclusions

HRL Hitachi Research Laboratory

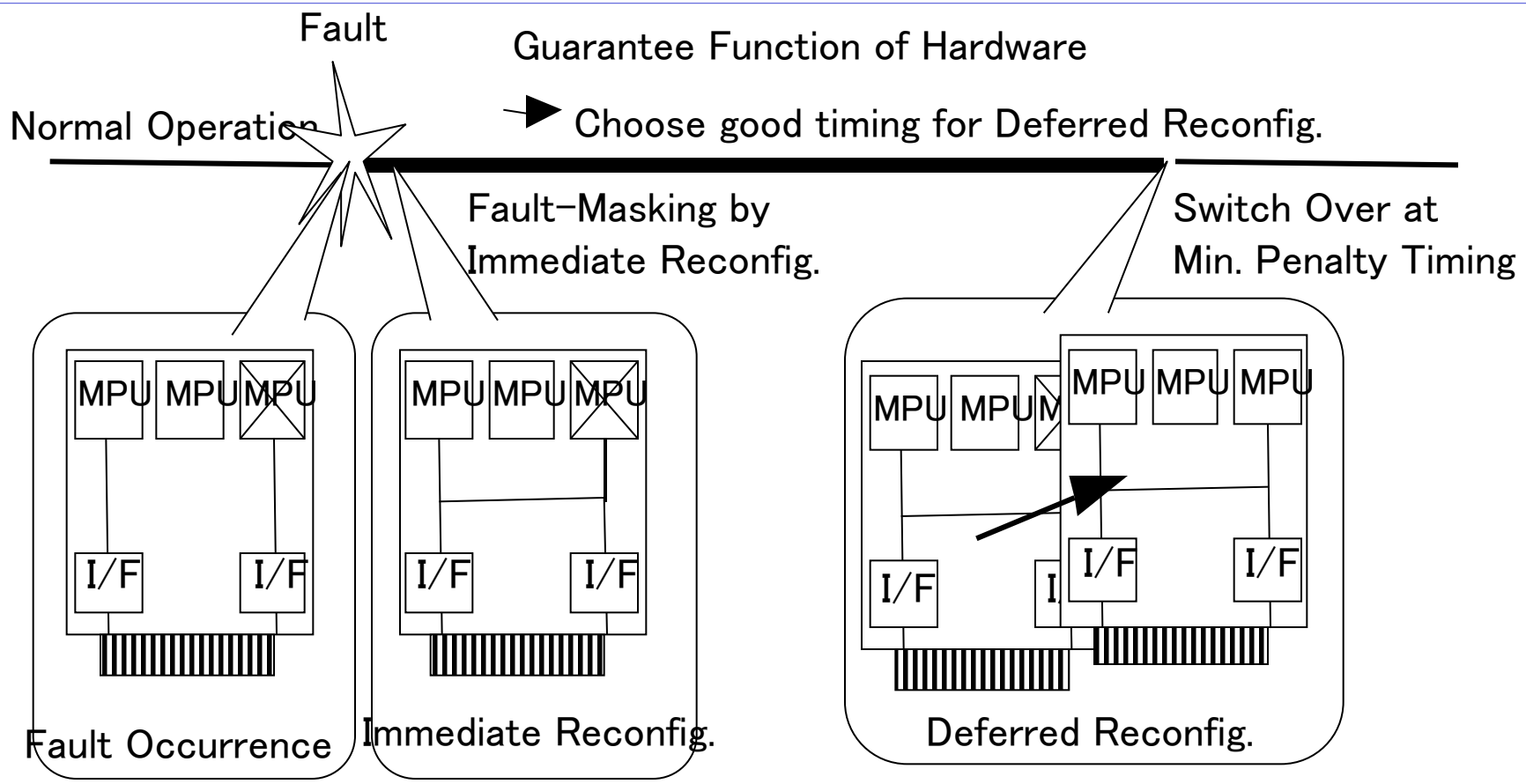
Synchronization and Overhead



Intra-Board Redundancy



Immediate/Deferred Reconfiguration

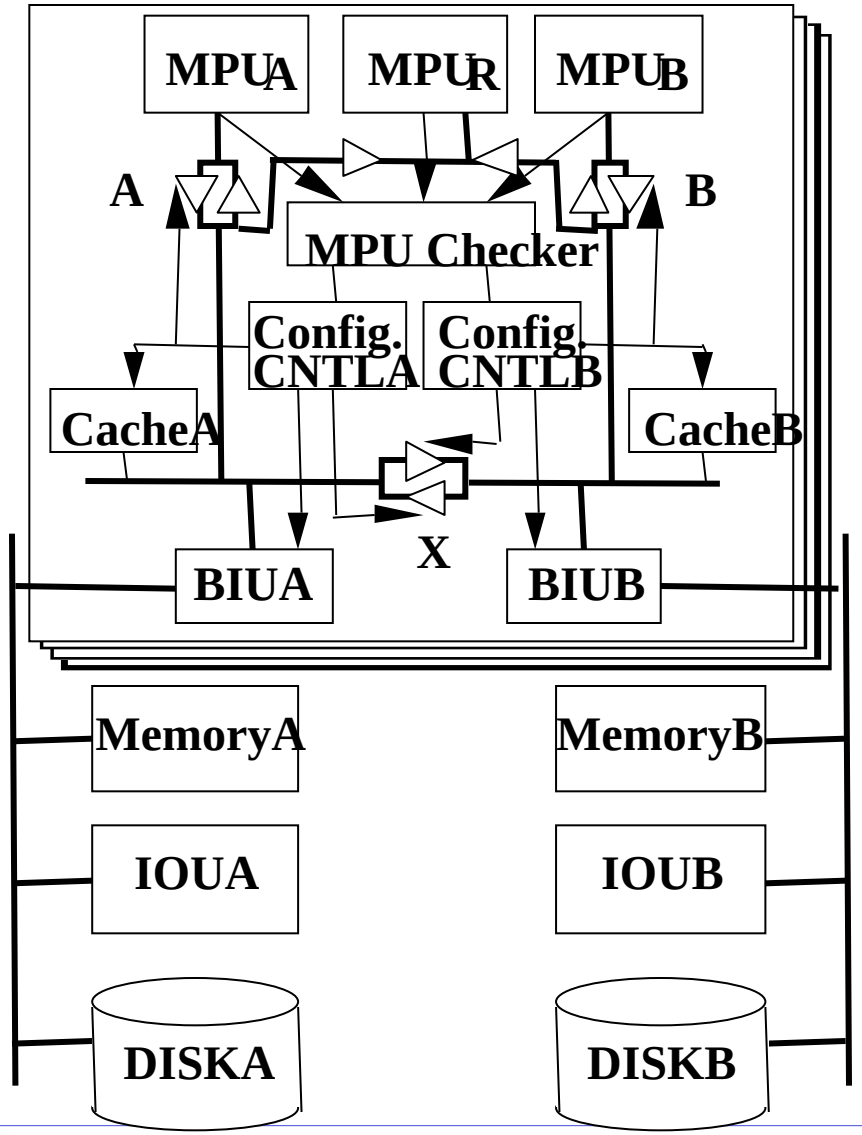


Immediate Reconfig. : Simple, First-Aid Reconfiguration by Hardware
Guarantee Function of Hardware

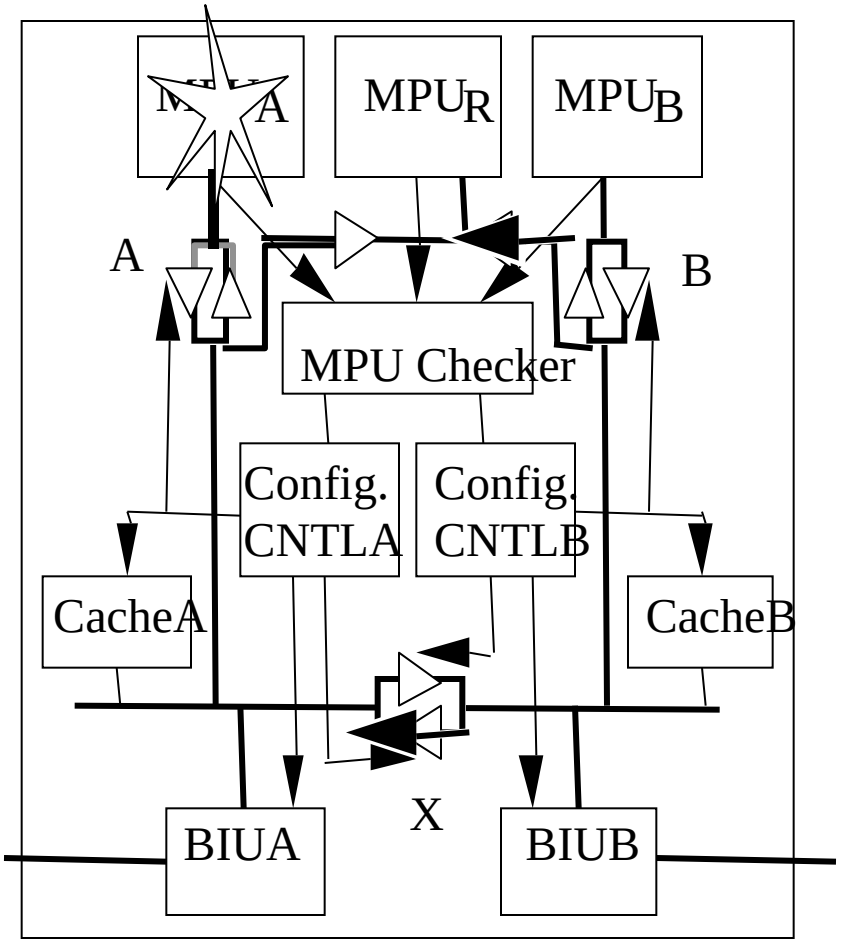
Deferred Reconfig. : Complex Reconfiguration by Software
Simplify Hardware

TPR Architecture

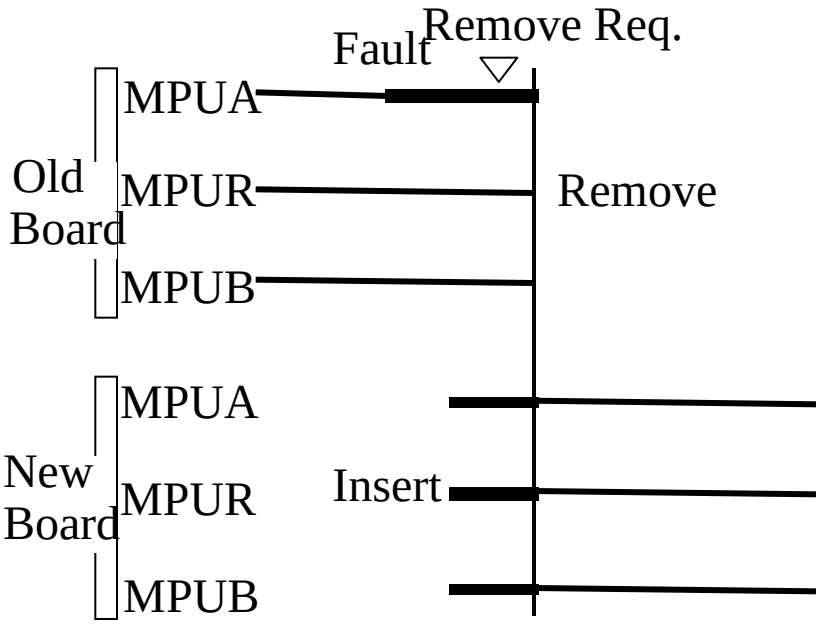
*Triple Processor & check Redundancy



Immediate/Deferred Reconfiguration



Immediate Reconfiguration



Deferred Reconfiguration

FT-6100

TPR Architecture

3500/FT

QPR Architecture

HITACHI
Inspire the Next

Contents

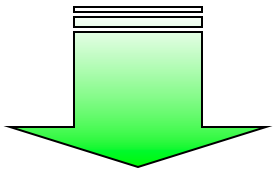
HRL Hitachi Research Laboratory

On-chip Redundancy

HITACHI
Inspire the Next

Integration of LSI →Needs for SEU Countermeasure
→Seeds for Multi-Core MPU

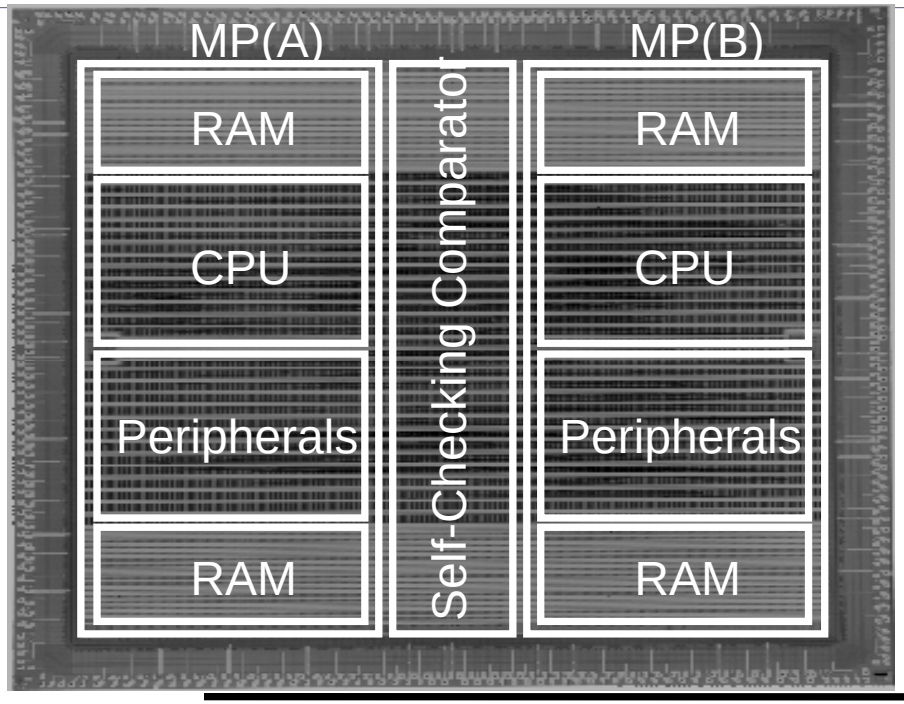
Electronic Control (Train Automotive)
→Needs for Dpendability

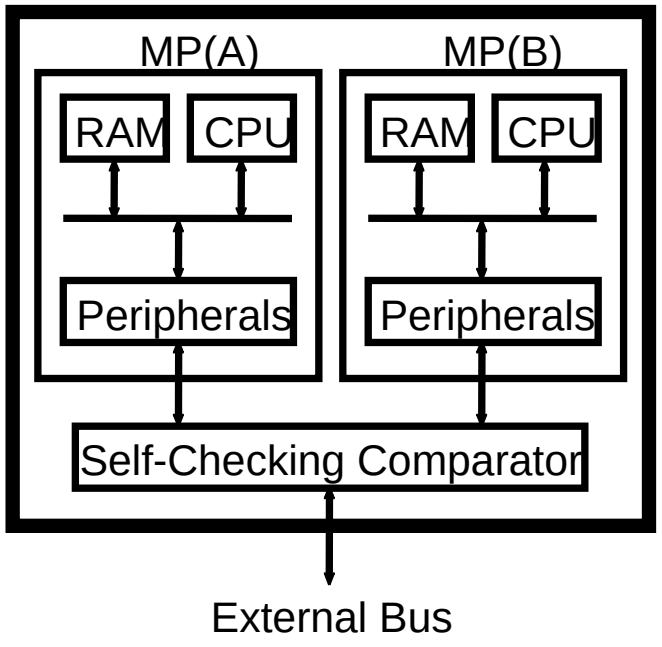


Safety Micro-controller (On-Chip Redudancy)

Safety Micro-Controller Prototype (FUJINE)

HITACHI
Inspire the Next





Process	0.35 µm 5 Metal CMOS
Hard Macros	PLL x 2, RAM(40KB)
Random Logic	740k gates
Chip Size	14.75 mm^2
Operating Frequency	60 MHz
Power Dissipation	2.6W @ 60MHz
Package	479pin BGA

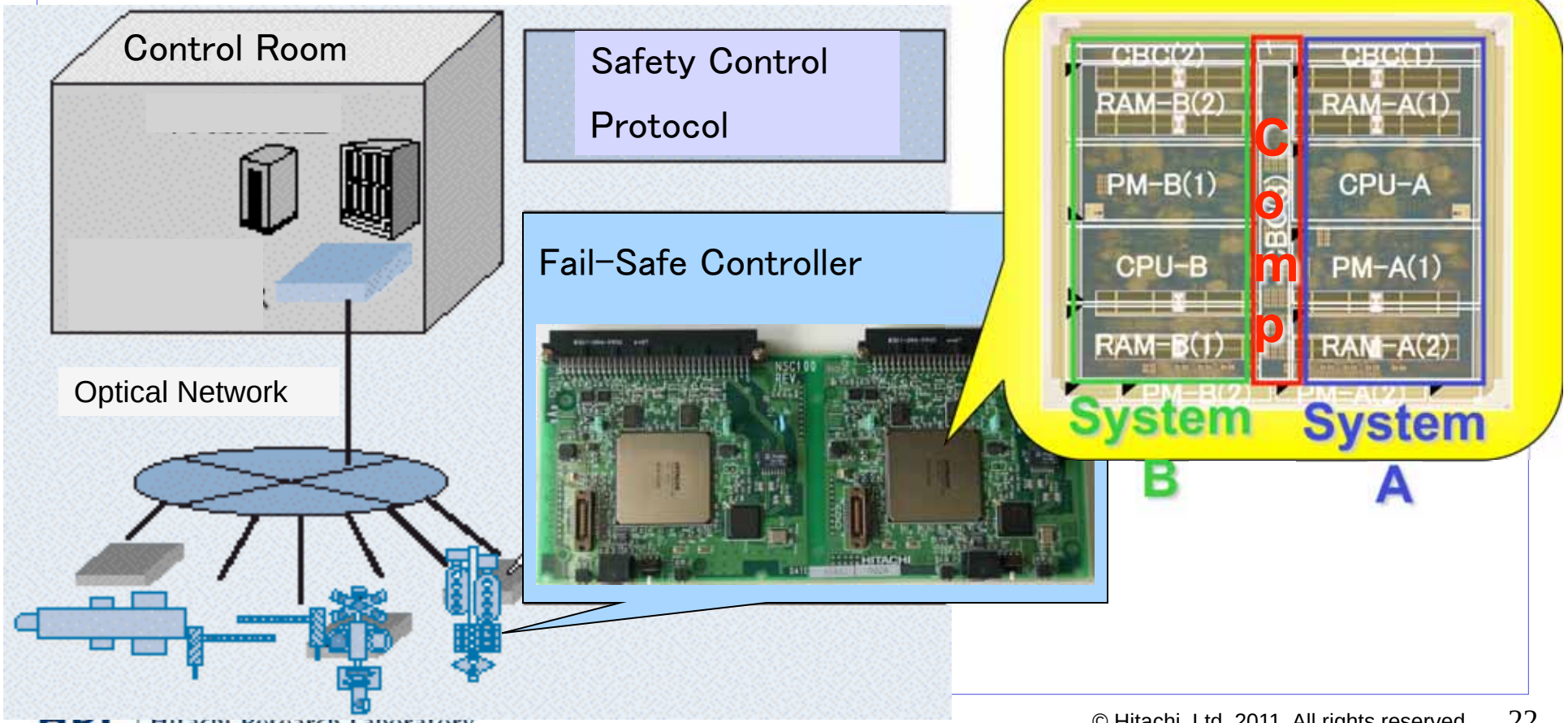
Safety Micro-Controller

HITACHI
Inspire the Next

1996 Frequency Logic(ATC-LSI)
1999 Prototype (FUJINE)
2006 Production Model

Small
Logic Size
Large

Integration
Soft IP Core

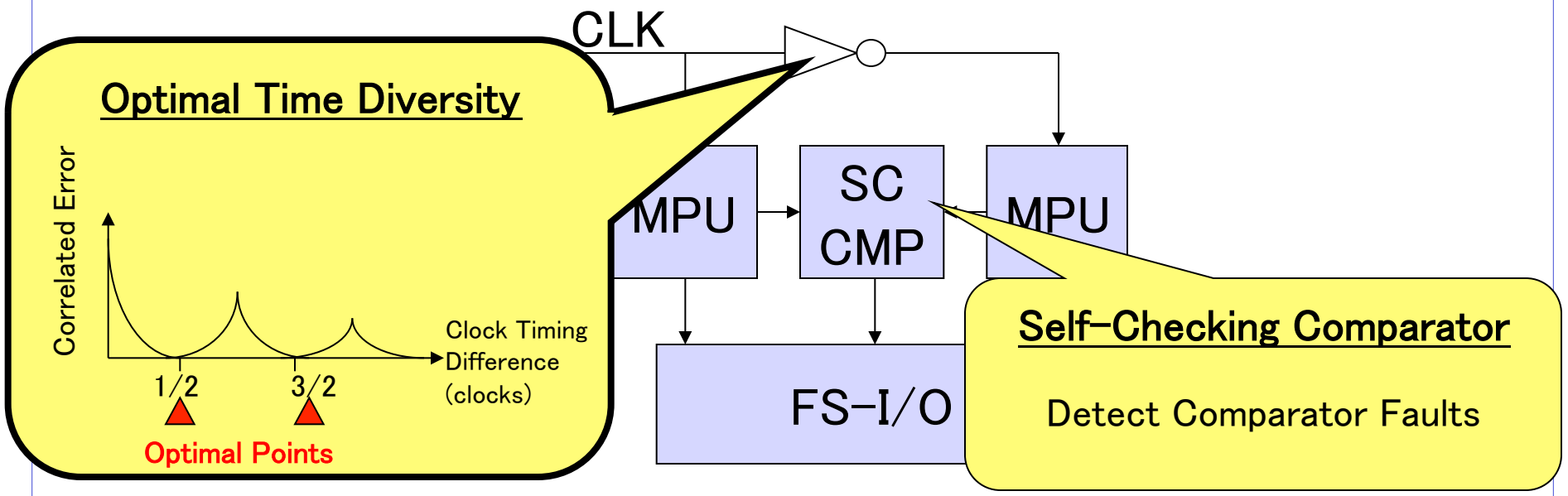


Self-Checking Processor

HITACHI
Inspire the Next

Error Detection by Lock-Step Dual

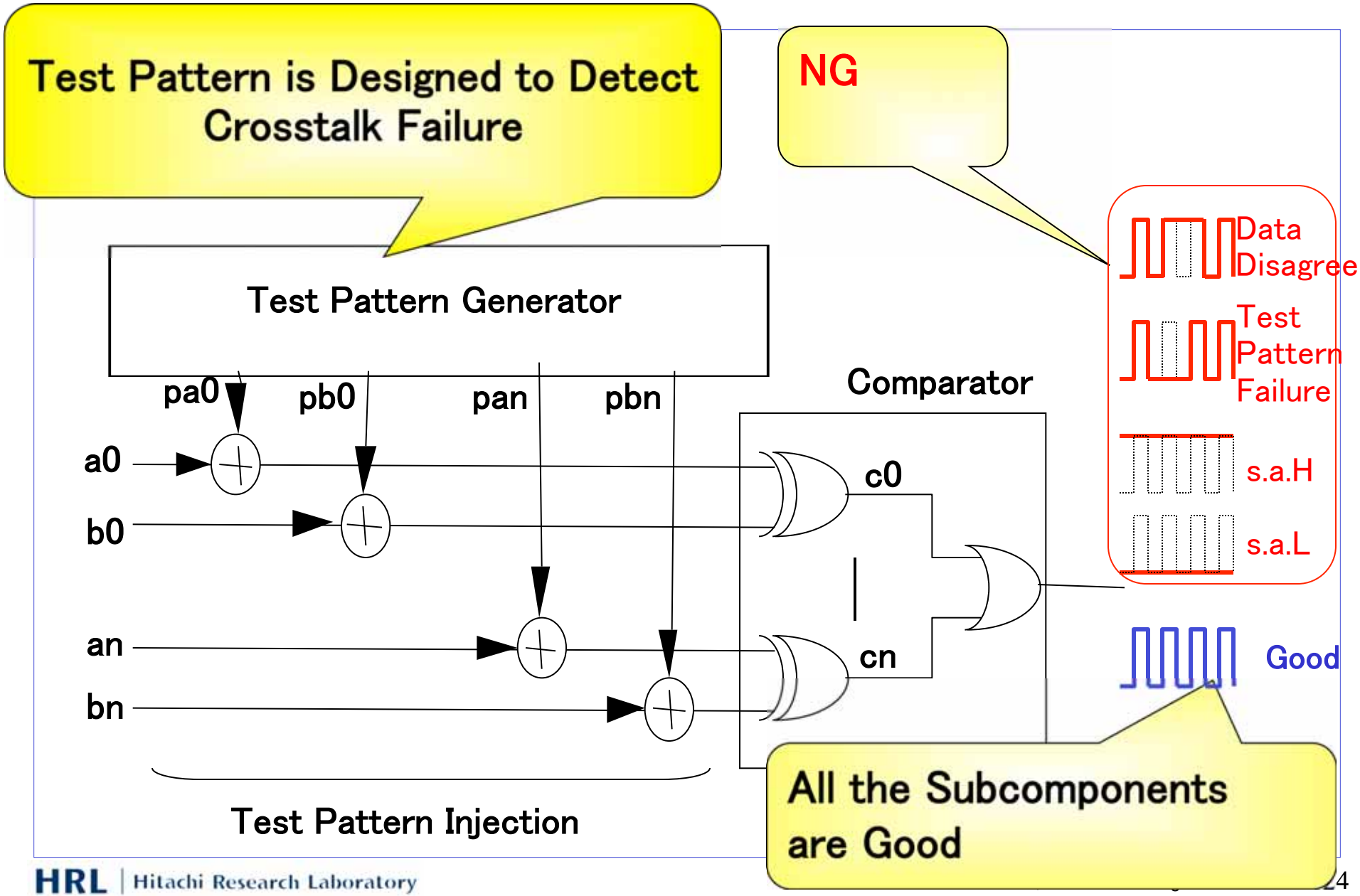
- **Comparator Failure→Mis-Detection**
- **Correlated Error→ Mis-Detection**



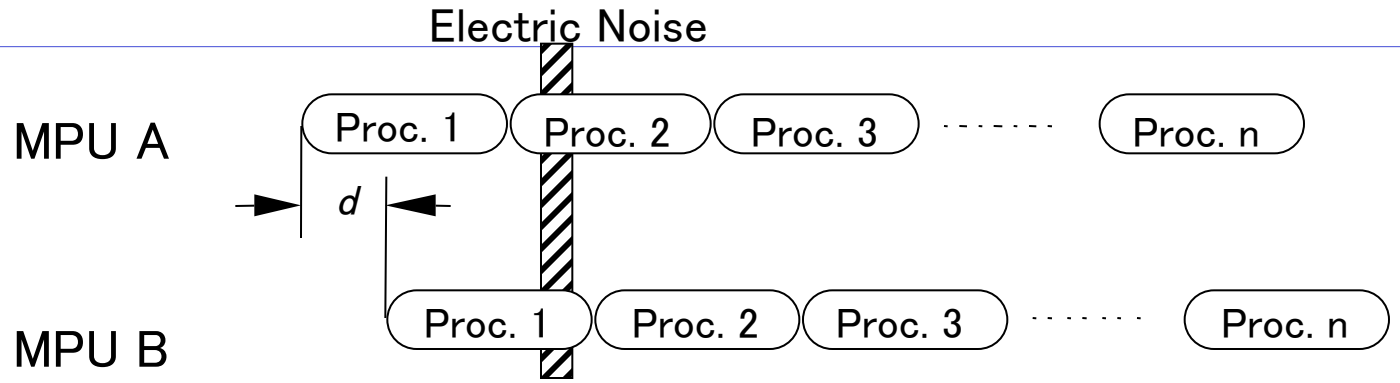
MPU:Micro-Processing Unit
SC:Self-Checking, FS:Fail-Safe
CMP:Comparator

Self-checking Comparator

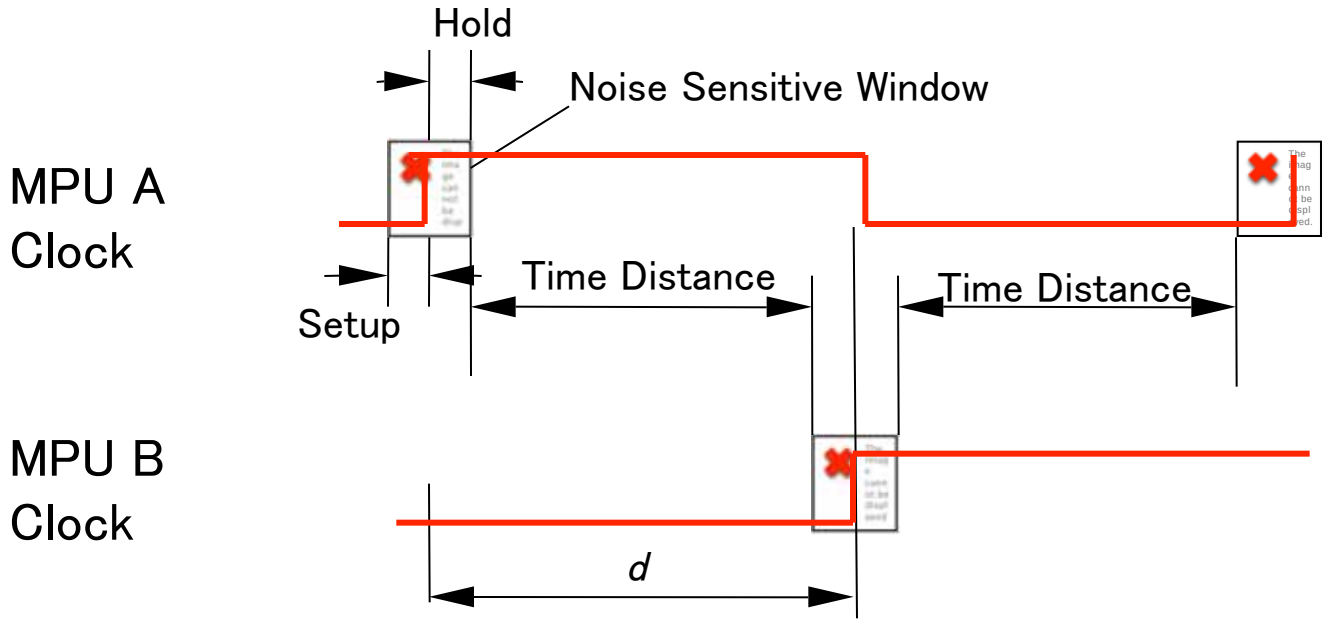
HITACHI
Inspire the Next



Effect Of Time Diversity

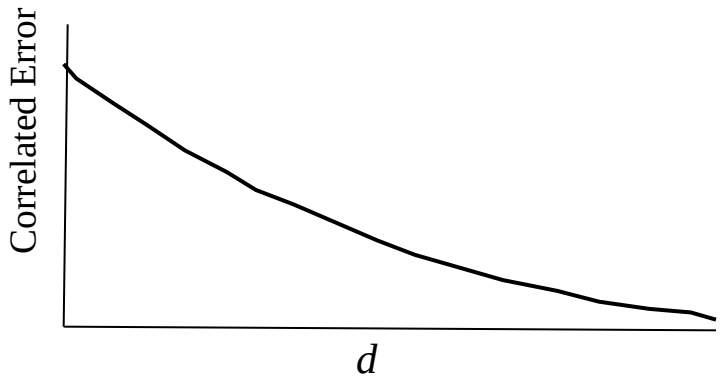


(a) Macro Effect.



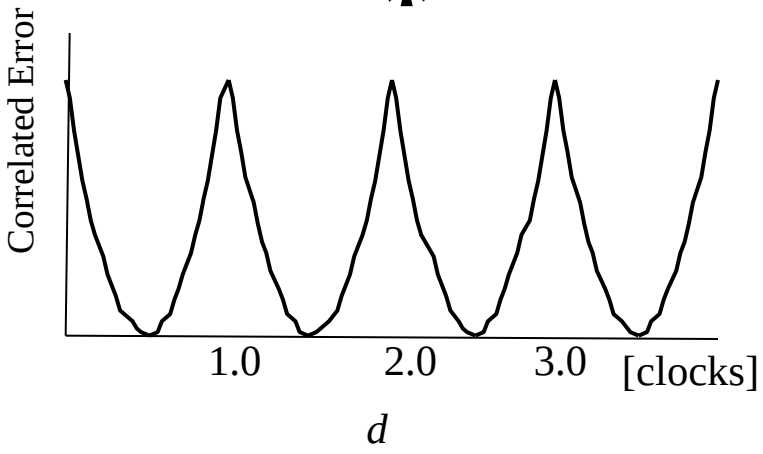
(b) Micro Effect

Effect Of Time Diversity

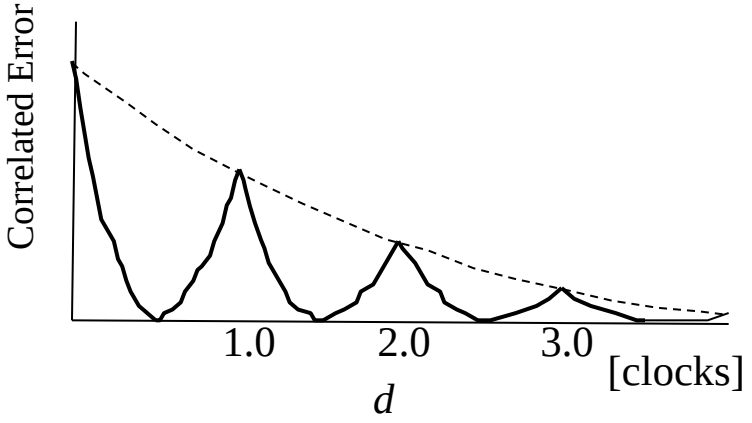


(a) Macro Effect

*

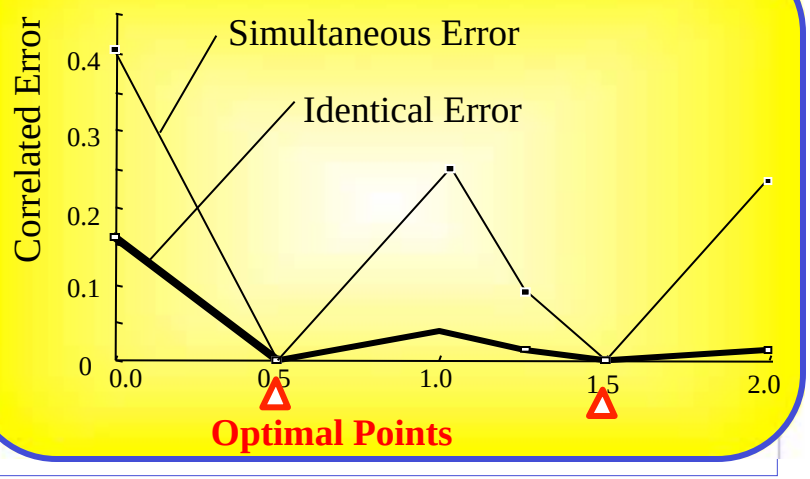


(b) Micro Effect



Overall Effect

Experimental Result



HITACHI
Inspire the Next

Contents

HRL Hitachi Research Laboratory

Conclusions

HITACHI
Inspire the Next

Integration of Semiconductor along with Moore's Law Causes;
- Terrestrial Neutron induced SEU's
- Synchronization Problem
- Electro-Magnetic Disturbance Sensitivity

Prospective Remedies;
- Intra-Board Redundancy
- On-chip Redundancy, and
- Consideration for Electro-Magnetic Disturbances (EMC, Power Integrity)

Reference includes Consideration for Electro-Magnetic Disturbances;

Kanekawa et al., "Dependability in Electronic Systems: Mitigation of Hardware Failures, Soft Errors, and Electro-magnetic Disturbances," Springer (2010)
ISBN-13: 978-1441967145

Hitachi's Expertise in Dependability

HITACHI
Inspire the Next

1960 1980 1990 2000

Nuclear Power

Main Flame

Autonomous Decetralized System

Space Computer

Steel
Manufacturing System

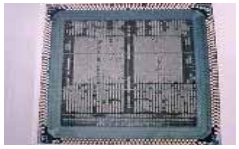
OLTP

FT-6100 3500/FT

Fly-by-Wire
Self-Checking

Train (Fail-Safe Technology)

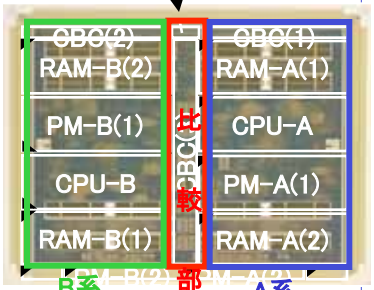
Stepwise Negotiating Voting
"Hiten"Onboard Computer



ATC
(Automatic
Train Controller)

Crossing Signal
Controller

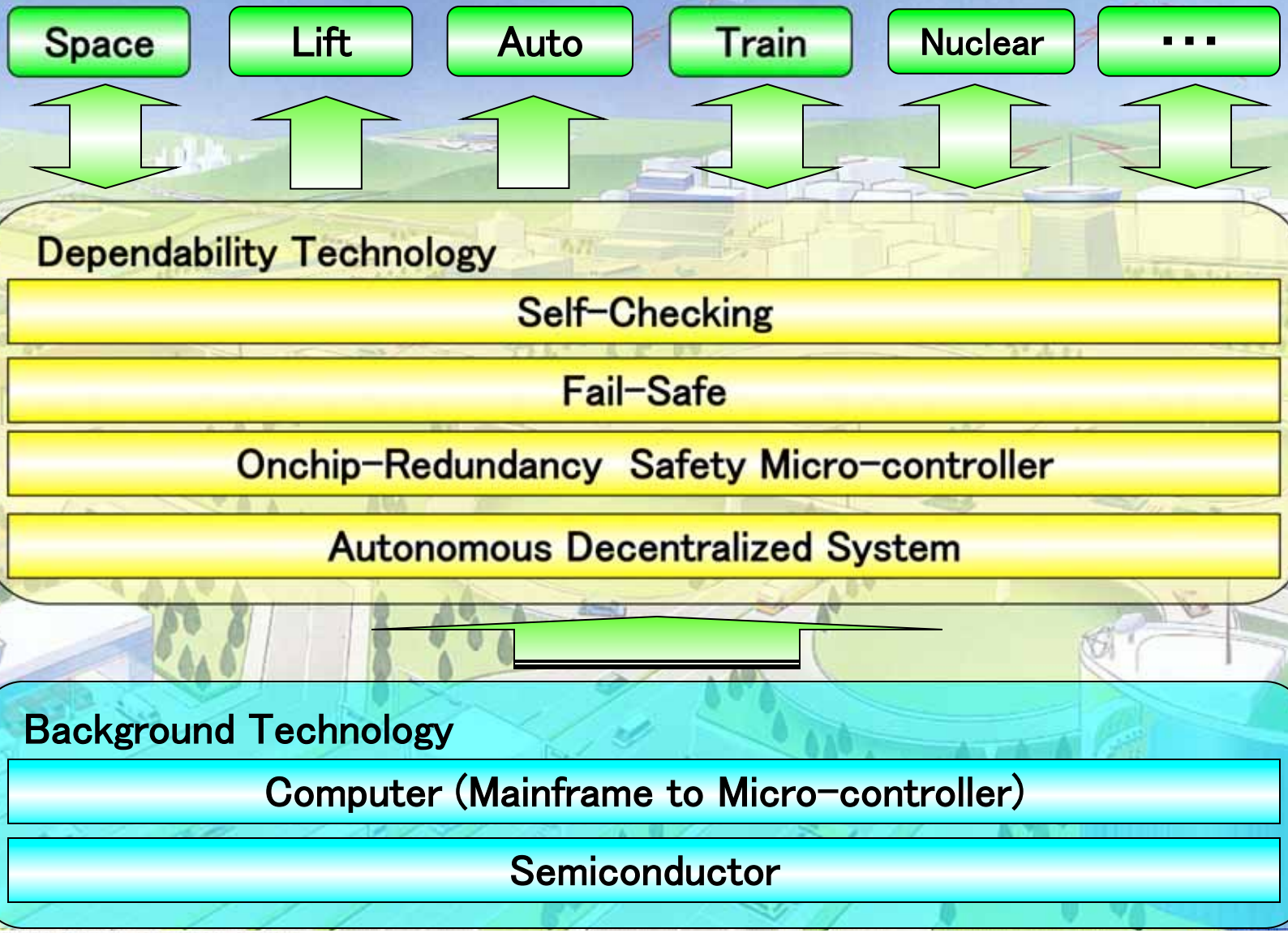
Train Control System



On-Chip
Redundancy

Hitachi's Approach for Dependability and Safety

HITACHI
Inspire the Next



HITACHI

Inspire the Next

“安心と信頼の日立”

in Taiwan