Wrap Up Session

Reports by Session Moderators

- Chuck Weinstock (Software Engineering Institute/CMU)
- Phil Koopman (Carnegie Mellon University)
- Bob Yeh (Boeing Commercial Airplanes)
- Luca Simoncini (University of Pisa)

Session 1: Emerging Hardware Development in Taiwan
Moderator: Chuck Weinstock

Hardware development in Taiwan is vibrant.

- Bruce Smith – IBM's ODM Development Model
  - Original Design Manufacturer involved in all phases of IBM's development process.
  - Often IBM designs start from an existing ODM design
- Rex Sung – Pegatron's Next Generation HPC Design Concept
  - Customer-oriented closed loop working model
  - Continuous customer feedback
- Shih-Chieh Chang – National Program for Intelligent Electronics
  - MG+4C (Medical, Green, Automotive, 3C Electronics)
  - As margins on existing businesses drop Taiwan is investing in new technologies to promote a leap of the Taiwan High Tech Industry
- Yen-Kuang Chen – Intel's Connected Context Computing
  - Connected Context Computing => smart devices collaborating. Context is important.
  - Devices are getting smaller and smarter. Biologic analogy. As species evolve they have better sensing and analysis capabilities.

Session 2: Hardware Architectures and Systems

Moderator: Phil Koopman

Hermann Kopetz (TU-Vienna)
System-level Error-handling Mechanisms in the Time-Triggered Architecture

- Overview of the Time Triggered Architecture (TTA)
- TTA Approach
  - Fundamental limits: data value quantization, time quantization, global synchronization frequency
  - Sparse time with ground state between processing cycles
  - Deterministic, uses a global time base
- Important ideas:
  - "Being faulty is normal"
  - Time triggered makes it easy to detect fail-silent
  - Partitioning, Isolation, other simplification strategies
  - Layered Fault Tolerance: Swift component recovery, on-chip TMR, off-chip TMR, Never Give up
  - Ground state gives a time for recovery/reintegration

Tomohiro Yoneda (National Inst. of Informatics)
Dependability Techniques for Networks on Chip

- Network on Chip
  - Key issues: Deadlock avoidance, on-line process, off-line process
- Packet routing (packets are multiple flits)
  - NoC different: small packets; low latency; high bandwidth; high reliability; restricted power consumption; simple/regular topology
  - Routing can be logic based (fast) or routing table (possibly slower)
- Faulty router → need a detour path
  - Might lose packets during reconfiguration
  - Need to fake end of packet to release path switches
  - Want to handle single and double fault cases
- Need deadlock avoidance in routing to enable concurrent packet movement
  - On-line reroute heuristics based on restricting order and types of movements (e.g., all negative transitions before positive transitions)
  - Off-line solutions can compute optimum alternative routing strategy

Rakesh Kumar (UIUC)
Stochastic Computing: Embracing Errors in Architecture and Design of Processors and Applications

- Computing with Stochastic Processors
  - Parameter variations are too high to limit chips to only using worst-case parameters
  - Want to expose component non-determinism to software; permits relaxing margins
- Modify hardware design and permit a small, limited number of errors
  - Don't want a steep slack wall
  - Can design to have some negative slack as voltage scales, with a target maximum error rate
  - Increase the slack of near-critical paths to reduce slack wall
  - Key idea: Optimize frequent near-critical paths; de-optimized infrequent near-critical paths
  - Yields power savings to hit any given error rate
  - Architectures optimized to have target error rates are different from (and can achieve lower power than) conventional architectures if you add HW
- Fault tolerant algorithms to deal with that limited number of errors
  - Reformulate as an optimization problem where correct answer is the minimum; solve for the minimum; example given for sorting
  - Current challenge is finding ways to reformulate wider variety of problems (or key pieces of problems) using "robustification" techniques.

Session 3: Hardware-related Fault Pathologies

Moderator: Bob Yeh

… and their Challenges for the High Integrity Systems and Networks, considering:

- Enabling Technologies and Algorithms
  - Sensors, Networks, Actuators, Massive Data Processing
- Threat for super-critical embedded control systems such as commercial airplanes Fly-By-Wire Computers:
  - Unknown failure modes
  - Soft & hard failures due to signal integrity
  - Soft & hard failures due to single event upsets/effects
- High Integrity Triple Channels systems remain viable for future increase of hardware Latch in Processors and Memory

Michel Renovell on Testing for Realistic Spot Defects in CMOS

- Classic Fault Model (FM):
  logic level fault simulation/testing
- Defect with realistic FM: electrical parameter
  vs threshold
- Defect with probabilistic FM
- Defect with statistical FM

- Comments:
  - Should the confidence level of statistical FM be evaluated?
  - Not all companies have seen value with bridging

Nobuyasu Kanekawa on Fault Pathologies Caused by Moore's Law

- Intra-Board Redundancy
  - Immediate Reconfiguration
  - Deferred Reconfiguration
- On-Chip Redundancy: Safety Micro-controller with Self-Checking Comparator
  - The concept has been developed for train controls systems with a MPU at 60 MHz.

Subhasish Mitra on Robust Systems for Scaled CMOS

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- Low cost resilience to soft error
  - BISER (built-in soft error resilience) achieves 2,000 fewer errors vs D flip-flop
  - LEAP (layout by error aware transistor positioning)
- Software-orchestrated global optimization is a MUST

—> On-line self-test and diagnostics

- Major Barrier of Carbon Nanotube FET
  - Mis-positioned CNTs
  - Metalic CNTs

Alan Wood on System Level Issues

- SEU rates decreases as feature sizes are reduced with exception of the 65 nm to 40 nm transitions.

- Retry instead of active redundancy

Session 4:
Assessment Methods and Techniques

Moderator: Luca Simoncini

Ching-Long Wei (National Central University, Taiwan) presented the IC design environment and chip implementation services of CIC

- The audience could taste the impressive effort that Taiwan is doing in high technology and the support that CIC provides to local universities.
- Possible co-operations are open to interested international partners.

Johan Karlsson (Chalmers University, Sweden) presented a study on the use of fault-injection-based assessment of SW FT mechanisms for dealing with HW faults

- He started by the observation that SW and system designers need to take into consideration HW faults.
- The idea is to try to transform critical failures into benign failures, taking advantage that many errors due to HW transient faults disappear or are detected by SW.
- His group experimented the influence that classical programming and Aspect Oriented Programming languages and the level of optimization of compilers have on the ability to mask or detect errors due to HW faults. The numbers produced showed that this approach is viable and if properly applied can help in increasing the dependability of systems.
- **Comments** were made on the confidence level of the numerical result obtained.

Ravi Iyer (UIUC, USA) dealt with the topic of HW support for reliability and security

- He started with a short history of the dependability supports since 1970 to today. While in the 70's, it was the time of large mainframes with a small number of highly trained people using computers, while today we have a multitude of connected smart devices and PDAs with millions of users worldwide with little or none experience.
- He stated that with ubiquitous computing, outages cannot longer be ignored, but there are growing costs for commodity systems. Since these systems fail and present decreasing feature size, this brings the reliability concern to the device level.
- The idea is that new low-cost techniques tailored to the specific needs of the application are required. Therefore the proposal is to insert at the application level, for each specific application, SW assertions that can be used as a low-cost mechanism for supporting reliability and security.
- **Comments** were made on the fact that present day systems are no more only technical, but are socio-technical and this requires a concerned approach to deal with what is offered to the multitude of consumers, trying to avoid the false impression that some sort of support for dependability may strenghten the myth of the infallibility of computers. Also it was noticed that reliability and security of socio-technical complex networked systems require contributions coming from other fields like social sciences, ergonomics etc.