60th Meeting of IFIP WG10.4 on Dependable Computing and Fault Tolerance

July 1-4, 2011 — Jhong Li City, Taoyuan, Taiwan

Workshop Hardware Issues in Dependable and Secure Computing

Organizers:

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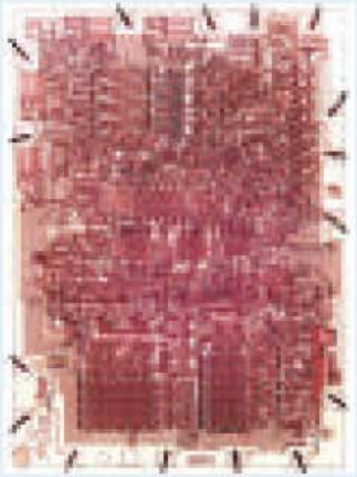
Saturday 2 & Sunday 3 July 2011

Hardware Technology Trends

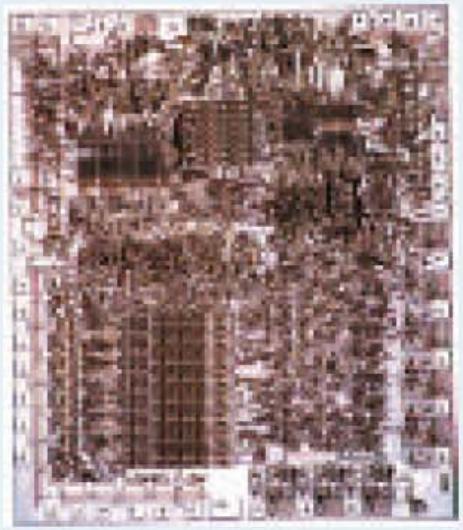
- Tracks towards nanoscale and future computing
  - Top Down (More Moore) — Shrinking CMOS technology devices
    ?? Increasing impact of variations in features
  - Bottom up (Beyond CMOS) — Self-assembling nanoscale elements
    ?? Signal amplification, selective control, …
  - Diversification (More than Moore) — Enhancing functionalities, Hybridation (SOCs, SIPs, MEMS)
    ?? Enhanced complexity, HW/SW-inclusive design, …
- In all cases, increased unreliability, higher susceptibility and even unpredictability, is to be expected…

Shekhar Borkar and Andrew A. Chien, "The Future of Microprocessors", CACM, May 2011, pp.67-77

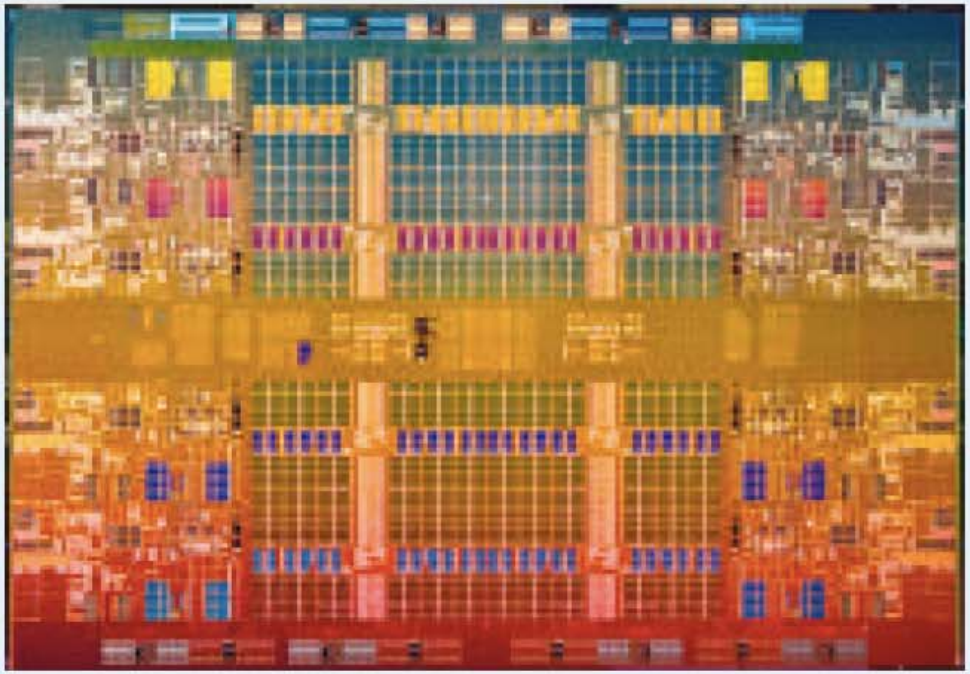
Figure 1. Evolution of Intel microprocessors 1971–2009.



Intel 4004, 1971
1 core, no cache
23K transistors



Intel 8088, 1978
1 core, no cache
29K transistors

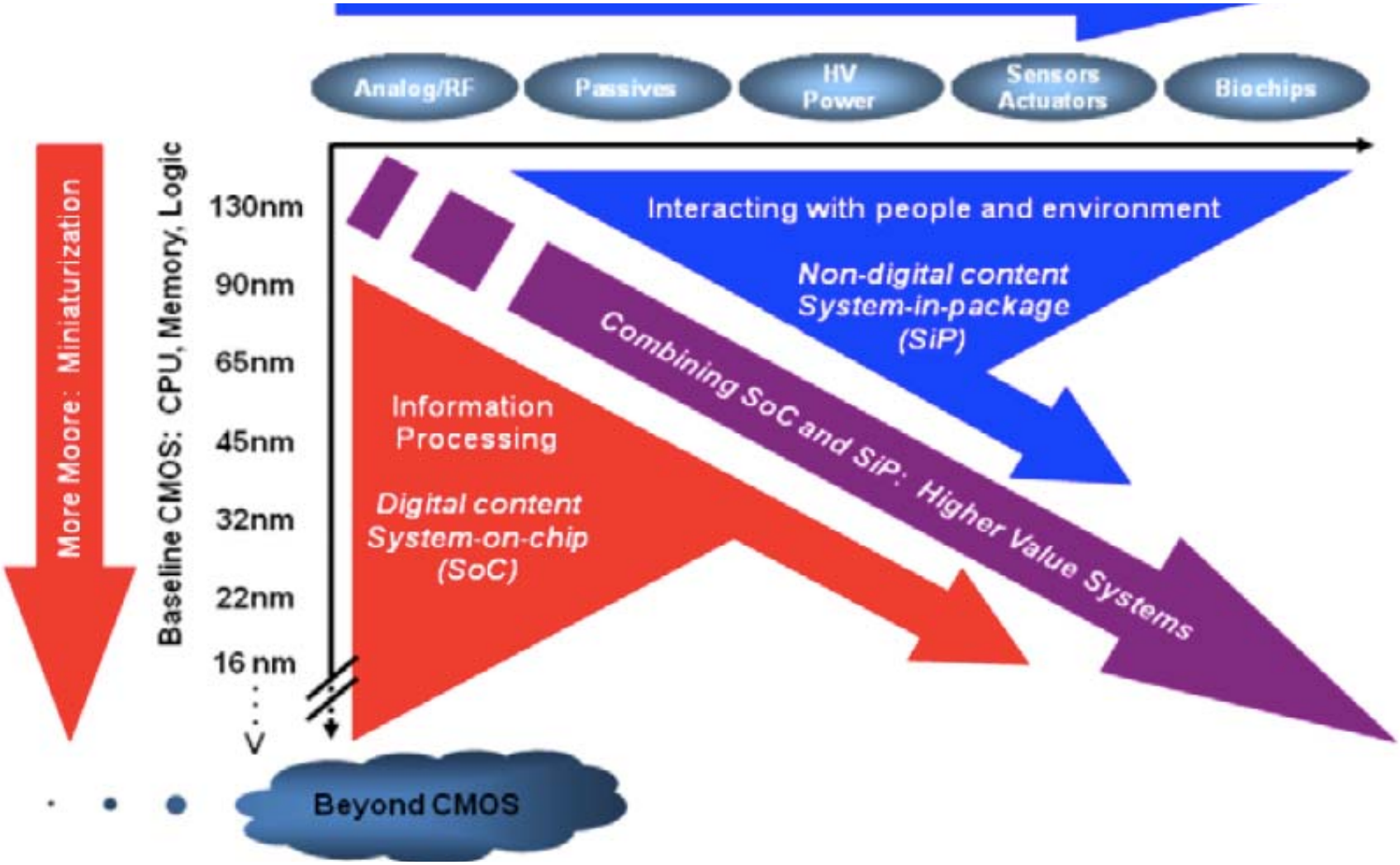


Intel Mehalem-EX, 2009
8 cores, 24MB cache
2.3B transistors

Some Further Rationale

- **ITRS** (International Technology Roadmap for Semiconductors)
  - 2008 Edition: Crosscutting Challenge 5: Reliability
  - 2009 Edition: Crosscutting Challenge 5: Reliability & Resilience
- **Quoting the Design Section** [http://www.itrs.net]
  - *Relaxing the requirement of 100% correctness for devices and interconnects may dramatically reduce costs of manufacturing, verification, and test.*
  - *Such a paradigm shift will likely be forced in any case by technology scaling, which leads to more transient and permanent failures of signals, logic values, devices, and interconnects.*
  - *In general, automatic insertion of robustness into the design will become a priority as systems become too large to be functionally tested at manufacturing exit.*
  - *Potential solutions include automatic introduction of redundant logic and on-chip reconfigurability for fault tolerance, development of adaptive and self-correcting or self-healing circuits, and software-based fault- tolerance.*

International Technology Roadmap For Semiconductors — 2010 Update

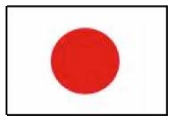


Emerging Services

- **Advances in hardware technologies**
  —> Development of embedded systems and unprecedented spread of pervasive computerized devices and services

Ubiquituous & Pervasive Computing

Ambiant Intelligence



Internet of Things

Even, more ☺:
Everyware, Smart Dust,
Haptic Computing,
Things that Think,
Cyber-Physical Systems,…

- **Enabling technologies and algorithms**
  —> Sensors, Communication networks, Actuators, Virtualization, Data processing,…
- **Wide range of services and applications**
  —> Health, Environment, Transportation, Energy,…
- **Threats**: Accidental and malicious faults!

About WDSN

Workshop on Dependable and Secure Nanocomputing

- 1st Edition at DSN-2007: Raising up the Awareness
- 2nd Edition at DSN-2008: Bringing up a Community
- 3rd Edition at DSN-2009: Link with IOLTS Community
  (42 attendees — 18 countries)
- 4th Edition at DSN-2010: Link with European Test Symp. Community (49 attendees — 9 countries)
- 5th Edition at DSN-2011: Strong participation of Asian Community

-> www.laas.fr/WDSNxx, xx ∈ {07,08,09,10,11}

Program-at-a-Glance

Moderator

1- Emerging Hardware Development in Taiwan ..... **Chuck Weinstock**
Bruce Smith, Rex Sung, Shih-Chieh Chang, Yen-Kuang Chen

2- Hardware Architectures and Systems ..... **Phil Koopman**
Hermann Kopetz, Tomohiro Yoneda, Rakesh Kumar

3- Hardware-related Fault Pathologies ..... **Bob Yeh**
Michel Renovell, Nobuyasu Kanekawa, Subhasish Mitra, Alan Wood

4– Assessment Methods and Techniques ..... **Luca Simoncini**
Ravi Iyer, Johan Karlsson, Chin-Long Wei

Wrap-Up ..... **All**