# **Application-Aware Security**

#### **Zbigniew Kalbarczyk**

W. Healey, K. Pattabiraman, R. Iyer

Center for Reliability and High-Performance Computing Coordinated Science Laboratory University of Illinois, Urbana-Champaign

- Detectors based on application-specific properties
- Early detection of attacks
  - Detect attacks before they corrupt critical memory state
- Derive detectors automatically from application
  - Extract properties of the application using compiler analysis
  - Enforce extracted properties at runtime
- Provide efficient hardware implementation
  - Integration with Reliability and Security Engine (RSE)
  - Low-latency monitoring and detection at runtime

### **Derivation of Attack Detectors**

- Goal: Preemptively protect "security-critical data"
- Technique: Information Flow Signatures
  - Derive dependences for critical variable using static analysis
  - Encode dependencies for critical variable(s) as signature
  - Check that the signature is not violated at runtime
- Can be applied selectively to critical variables in program even though other variables are attacked
- Threat/Attack Model
  - Memory Corruption Attacks (Buffer overflows, format string)
  - Hardware attacks (smart-card based attacks)
  - Insider attacks (malicious plugins, third party libraries)

### **Attack Detectors: Conceptual Example**



Critical Variable: authenticated; Signature: {10,6},{3}

#### Level 1 Check: Trustedness



#### Level 2 Check: Verification of Trust



Level 2 : Each trusted instruction writes only to its allowed targets (as determined by compiler)

#### **Level 3 Check: Completeness**



### **Example Results for Attack Detectors: OpenSHH**

**Software Checking Overheads** 



Performance overhead depends on length of dependence trees of critical variables and the size of the set of allowed targets for trusted instructions



#### **Hardware Implmentation**

- FPGA implementation and sythesis of the Level 1 and Level 3 checks
- Performance overhead:
  - 4.8% (for OpenSHH, WuFTP, and NullHttpd)
- Hardware area overhead
  - 30% on FPGA (but only 7.5% of equivalent ASIC gates)
  - ASIC implementation routes not constrained to pre-placed wires (as it is on FPGA) and can be placed more efficiently



#### **Executing on a Coprocessor:** <u>The Trusted Illiac Node Architecture</u>

#### Trusted Illiac Node



## **Deployment in Trusted Illiac**



for advanced hardware development

Reliability and Security Engine •DLX (MIPS ISA) •Leon3 (SPARC ISA)

- Application-specific detectors
  - > Reliability process health monitor, data value checking
  - Security dataflow signature checking, pointertaintedness checking
- Definition of hardwaresoftware interfaces
  - P2P Streaming application
  - Model-driven trust management
- Integration of hardware accelerators with Linux OS