Platform Issues

- Building integrated HW platforms such as Blade Offerings exposes weaknesses and ad hoc nature of current web practices
  - Control points example:
    - Critical component (sensing and actuation)
    - Each subsystem/vendor has unique interface, little thought to survivability, security of interface (as if each system expected direct VT100 attachment to serial port)
  - Virtualization Concepts now immature – but essential for tractability
    - Processor/Memory (compute core) fairly advanced
    - Disk – there but interoperability and inconsistencies are just as bad as unvirtualized resources
    - Network – vendor tool specific
  - Fragments of solutions
    - Work Load Balancing, Software Rejuv, VLAN's, Virtual Machines (e.g., VMware)
    - Some critical pieces seem to have made progress
      - Initial bare metal provisioning is example
    - Much more needs to be done – lots of pieces means lots of manual work (the non-autonomic part of the problem) e.g., initial provisioning and patching often different tools
- Approach to achieving tractability and scalability elusive
  - Simplicity vs flexibility and complexity

Platform Issues

- Some consensus
  - “Service Processor” infrastructure seems a common feature
    - IBM, HP, Newisys all have service processors as key control component
    - The cluster of service processors and service processor redundancy not addressed
    - Security and manageability of service processor cluster needs to be addressed (are security attempt simply amateur, or are they effective)
  - Separating the disk from the computer core common theme
    - SAN and NAS attached storage
    - Magnifies management complexity issues – many difficult end-to-end problems.
  - Role of VLAN in multitier Web seemed:
    - Well understood
    - A complete mystery
    - Obviously critical security and control point

Platform Issues

- Some basic issues:
  - Pervasiveness of “Fail-Stop” assumptions
    - What design attributes are included and need to be included to back this assumption
      - Matched pairs for computational core for example
      - OS checking (never mind when the processor is brain dead, what about brain dead OS)
  - What are basic failure rates, failure modes, failure correlations
    - Lots of uncertainty going forward as:
      - Increasing circuit densities may or may not increase transient error rates
      - Critical SW failure rates and modes are unknown now with more uncertainty looking forward (e.g., how frequently does Windows fail and what fraction of those failures corrupt critical components of file system, or how frequently does firmware in RAID subsystem lose all the data in the RAID subsystem)
      - What about the backplanes in these integrated systems
      - How often does management subsystem mistakenly turn off all elements in system
      - What are the basic HW failure rates

Platform Composibility Issues

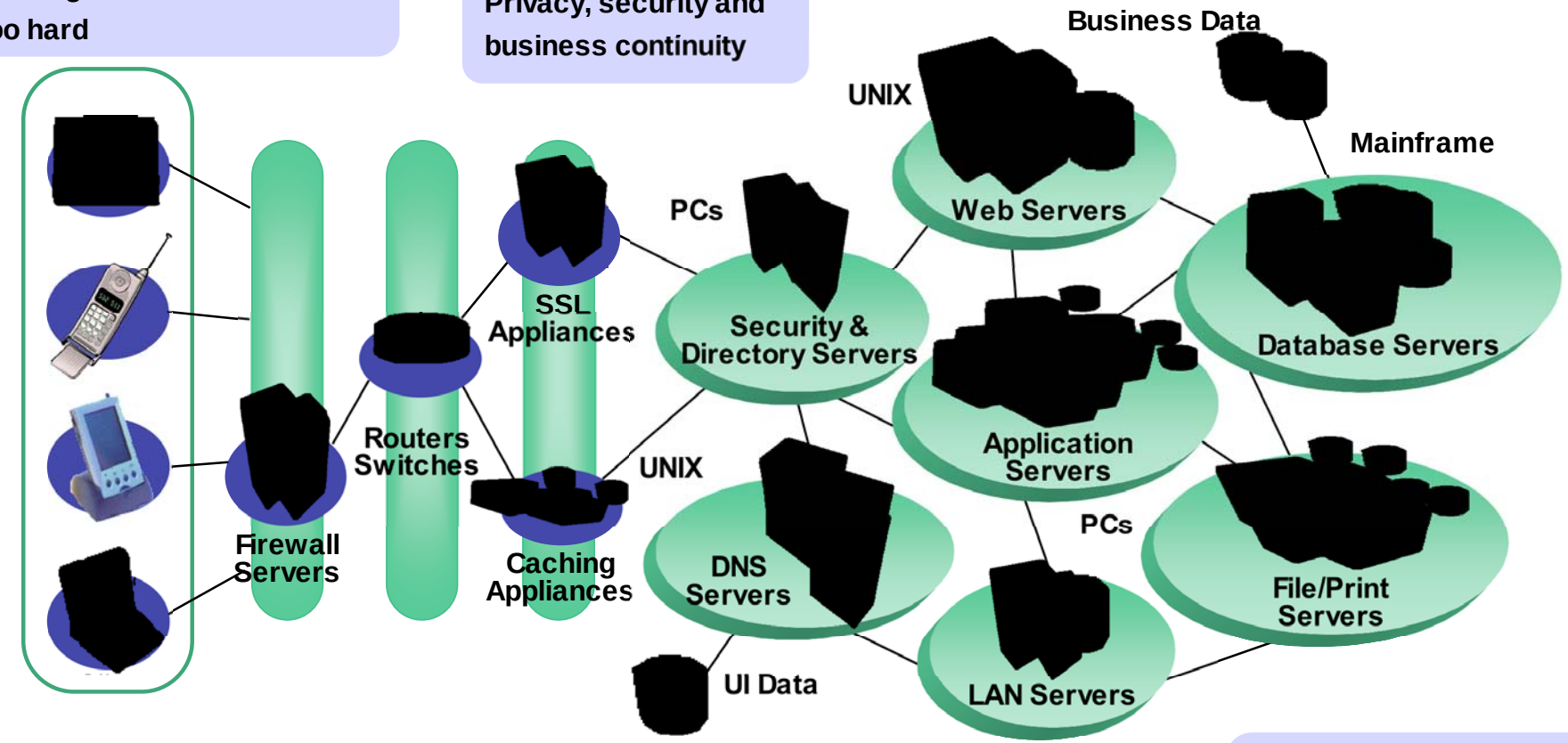
- General composibility problem with constrained perfectly virtualized resources is very hard (HP UDC made stab are regularizing resources – fixed wiring constraints)
  - With constraints this is still a form of classically impossible problem if best solution is required, even good is hard
- With general imperfectly virtualized resources things may be intractable

Autonomic Configuration of Complex Infrastructure

Management of complex, heterogeneous environments too hard

Privacy, security and business continuity

IT asset utilization is way too low



Operational speed too slow; IT flexibility too limited

Swamped by the proliferation of technology and platforms to support

Inability to manage the infrastructure seamlessly